



# **CrystalFontz America, Incorporated**

## GRAPHIC LCD MODULE SPECIFICATIONS



|                           |  |
|---------------------------|--|
| CrystalFontz Model Number | CFAG12864B-TMI-V   |
| Hardware Version          | Revision "A", September 2005   |
| Data Sheet Version        | Revision 1.0, December 2006  |
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| Customer Name             |  |
| Customer Part Number      |  |

### **CrystalFontz America, Incorporated**

12412 East Saltese Avenue  
Spokane Valley, WA 99216-0357

Phone: (888) 206-9720

Fax: (509) 892-1203

Email: [techinfo@crystalfontz.com](mailto:techinfo@crystalfontz.com)

URL: [www.crystalfontz.com](http://www.crystalfontz.com)



## REVISION HISTORY

| HARDWARE   |                              |
|------------|------------------------------|
| 2005/09/01 | Current Hardware Version: vA |

| DATA SHEET |                      |
|------------|----------------------|
| 2006/12/15 | New Data Sheet: v1.0 |

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## MAIN FEATURES

- ❑ 128 x 64 dots graphic LCD module has a large display area in a compact 75.0 (W) x 52.7 (H) x 8.9 (D) millimeter package (2.95" (W) x 2.07" (H) x .35" (D)).
- ❑ White edge LED backlit with STN negative transmissive mode LCD. Displays illuminated light dots on a blue background.
- ❑ Built-in controllers Samsung PN S6B0107B (formerly Samsung PN KS0107B, see [APPENDIX C: SAMSUNG S6B0107 64 CH COMMON DRIVER \(Pg. 28\)](#)) and Samsung S6B0108B (formerly Samsung PN KS0108B, see [APPENDIX D: SAMSUNG S6B0108 64 CH SEGMENT DRIVER \(Pg. 29\)](#)).
- ❑ 8-bit parallel interface.
- ❑ Wide temperature operation: -20°C to +70°C.
- ❑ RoHS compliant.

## MODULE CLASSIFICATION INFORMATION

CFA G 128 64 B - T M I - V\*

1 2 3 4 5 6 7 8 9

|          |  |   |
|----------|--|---|
| <b>1</b> | Brand  | CrystalFontz America, Inc.  |
| <b>2</b> | Display Type   | G – Graphic   |
| <b>3</b> | Number of Dots (Width)   | 128 dots  |
| <b>4</b> | Number of Dots (Height)  | 64 dots   |
| <b>5</b> | Model Identifier   | B   |
| <b>6</b> | Backlight Type & Color   | T – LED, white  |
| <b>7</b> | Fluid Type, Image (positive or negative), & LCD Glass Color              | M – STN negative, blue  |
| <b>8</b> | Polarizer Film Type, Wide Temperature (WT) Range, & View Angle (O’Clock) | I – Transmissive, WT, 6:00 <sup>1</sup>   |
| <b>9</b> | Special Code   | V – Built-in negative voltage generator (on the board)<br>*<br>– May have additional manufacturer's codes at this location. |

<sup>1</sup>For more information on View Angle, see [Definition of 6 O’Clock and 12:00 O’Clock Viewing Angles \(Pg. 15\)](#).



## ORDERING INFORMATION

| PART NUMBER  | BUILT-IN NEGATIVE VOLTAGE GENERATOR | FLUID | LCD GLASS COLOR | IMAGE    | POLARIZER FILM | BACKLIGHT              |
|--|-------------------------------------|-------|-----------------|----------|----------------|------------------------|
| CFAG12864B-TMI-V   | Yes                                 | STN   | blue            | negative | transmissive   | white edge LEDs        |
| <i>Additional variant (same form factor, different LCD mode or backlight):</i> |                                     |       |                 |          |                |                        |
| CFAG12864B-TFH-V   | Yes                                 | FSTN  | light           | positive | transflective  | white edge LEDs        |
| CFAG12864B-WGH-N   | No                                  | STN   | light           | positive | transflective  | white EL lamp          |
| CFAG12864B-WGH-V   | Yes                                 | STN   | light           | positive | transflective  | white EL lamp          |
| CFAG12864B-YYH-N   | No                                  | STN   | yellow-green    | positive | transflective  | yellow-green edge LEDs |
| CFAG12864B-YYH-V   | Yes                                 | STN   | yellow-green    | positive | transflective  | yellow-green edge LEDs |

## MECHANICAL SPECIFICATIONS

---

### PHYSICAL CHARACTERISTICS

| ITEM              | SIZE                             |
|-------------------|----------------------------------|
| Number of Dots    | 128 x 264 dots                   |
| Module Dimensions | 75.0 (W) x 52.7 (H) x 8.9 (D) mm |
| Viewing Area      | 60.0 (W) x 32.6 (H) mm           |
| Active Area       | 55.0 (W) x 27.48 (H) mm          |
| Dot Size          | .39 (W) x .39 (H) mm             |
| Dot Pitch         | .43 (W) x .43 (H) mm             |
| Weight            | 36 grams (typical)               |



# MODULE OUTLINE DRAWING

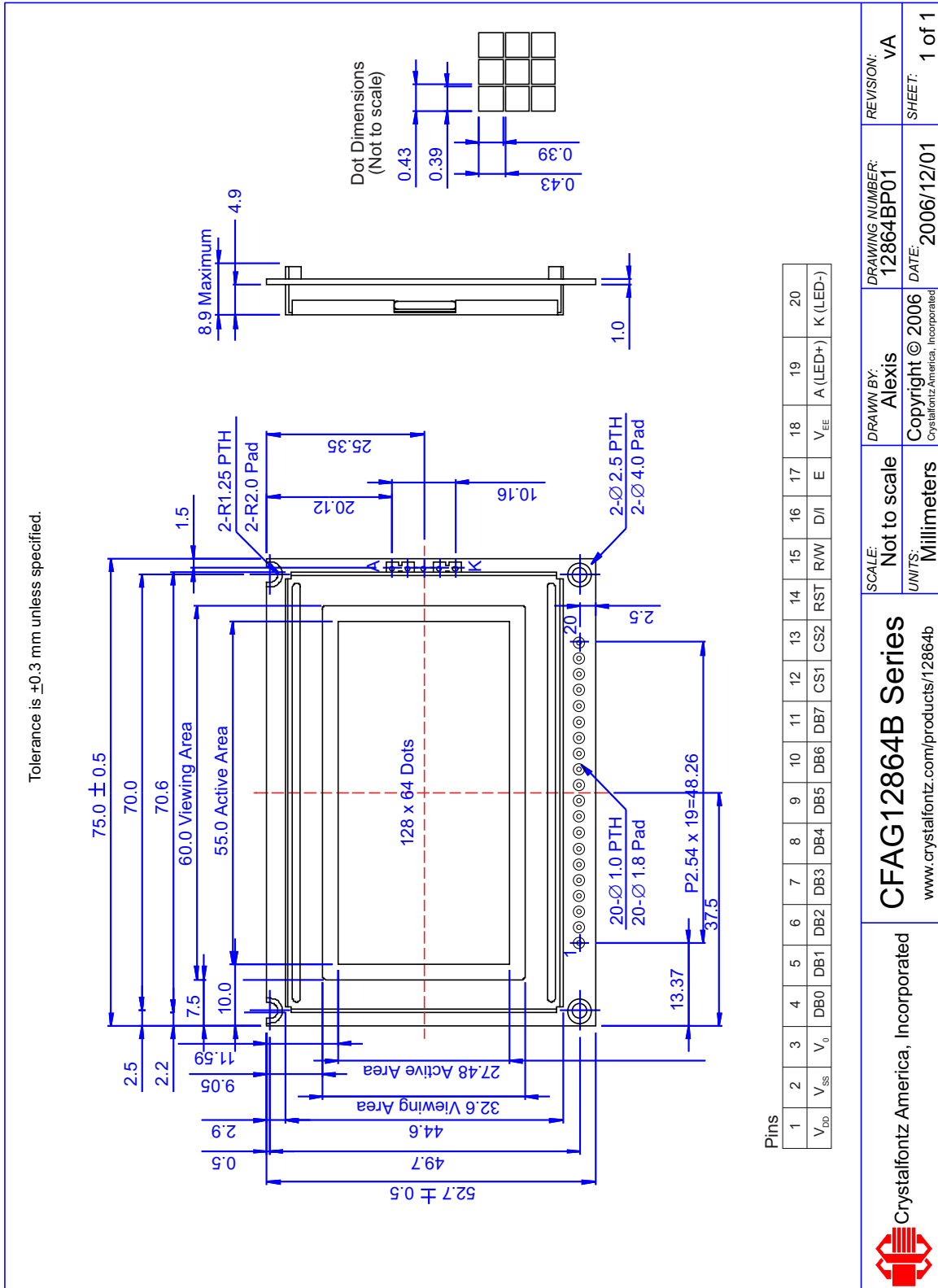
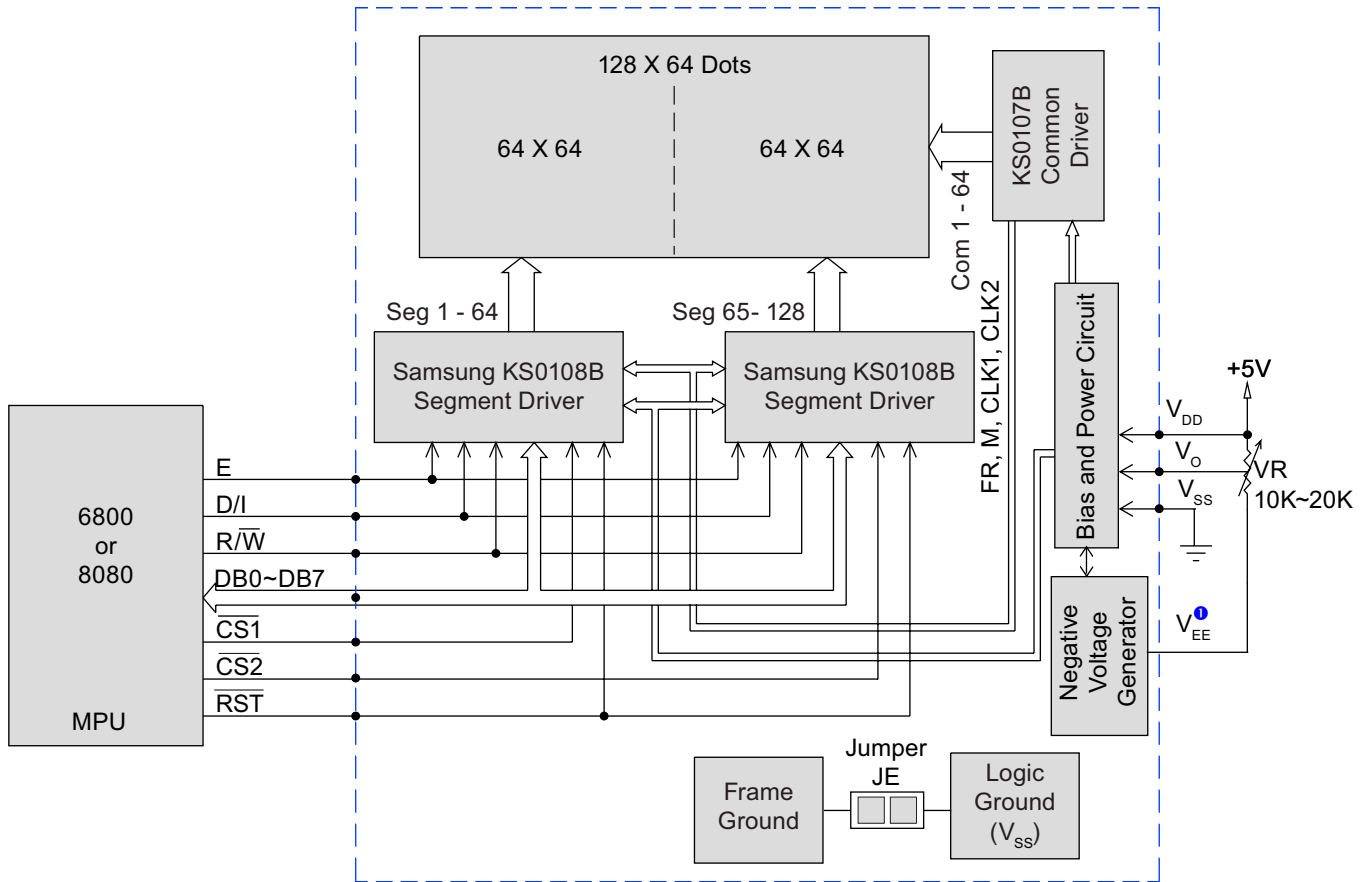


Figure 1. Module Outline Drawing



# ELECTRICAL SPECIFICATIONS

## SYSTEM BLOCK DIAGRAM



<sup>1</sup>V<sub>EE</sub> = output pin of on-board negative voltage generator

Figure 2. System Block Diagram





## FRAME GROUND

Frame Ground (shown in the System Block Diagram above) is a trace that connects some of the bezel tabs. To connect Frame Ground to the Logic Ground ( $V_{SS}$ , Pin 2), use an "0805" package 0 ohm resistor to close jumper **JE**.

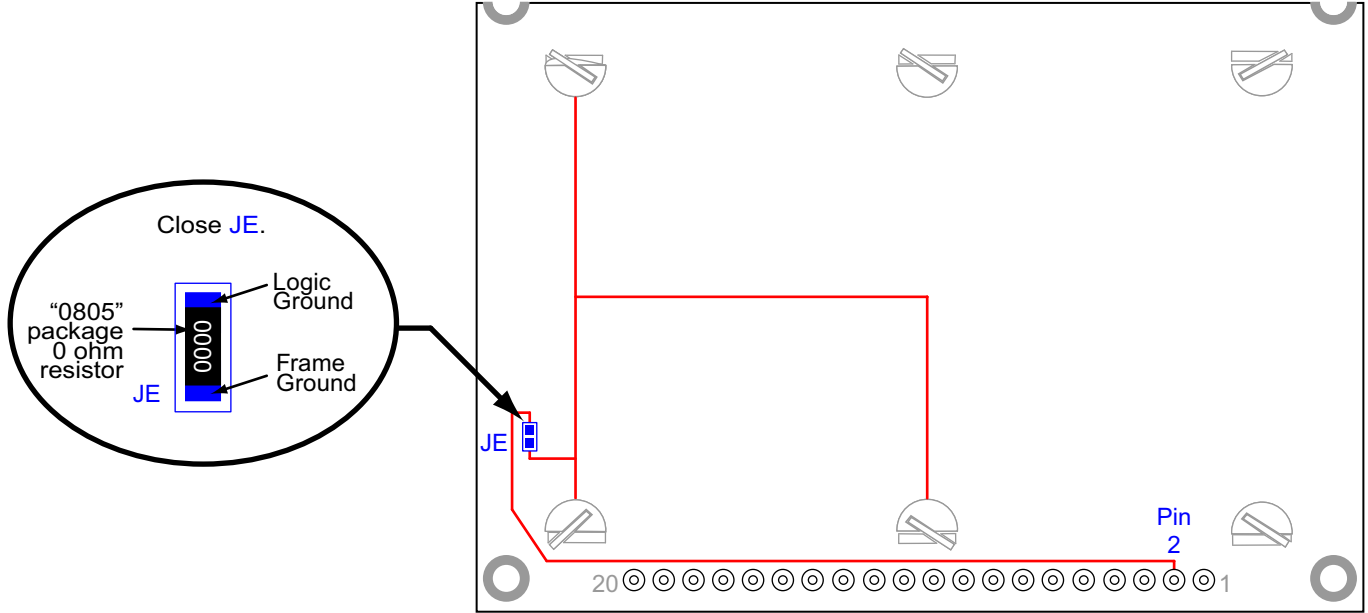


Figure 3. Frame Ground (Back View of Module)



## DRIVING METHOD

| DRIVING METHOD | SPECIFICATION |
|----------------|---------------|
| Duty           | 1/64          |
| Bias           | 1/9           |

## ABSOLUTE MAXIMUM RATINGS

| ABSOLUTE MAXIMUM RATINGS | SYMBOL                          | MINIMUM | MAXIMUM         |
|--------------------------|---------------------------------|---------|-----------------|
| Operating Temperature    | T <sub>OP</sub>                 | -20°C   | +70°C           |
| Storage Temperature*     | T <sub>ST</sub>                 | -30°C   | +80°C           |
| Input Voltage            | V <sub>I</sub>                  | 0       | V <sub>DD</sub> |
| Supply Voltage for Logic | V <sub>DD</sub>                 | 0       | 6.7v            |
| Supply Voltage for LCD   | V <sub>DD</sub> -V <sub>O</sub> |         | 16.0v           |

*\*Note: Prolonged exposure at temperatures outside of this range may cause permanent damage to the module.*

## DC CHARACTERISTICS

| DC CHARACTERISTICS*                                  | SYMBOL   | MINIMUM                | TYPICAL | MAXIMUM         |
|--|--|------------------------|---------|-----------------|
| Supply voltage for driving LCD                       | T <sub>A</sub> = -20°C<br>V <sub>DD</sub> - V <sub>O</sub> |                        |         | +9.8v           |
|  |  | T <sub>A</sub> = +25°C | +8.0v   |                 |
|  |  | T <sub>A</sub> = +70°C | +7.6v   |                 |
| Logic Voltage  | V <sub>DD</sub>  | +4.5v                  | +5.0v   | +5.5v           |
| Input High Voltage                                   | V <sub>IH</sub>  | 3.5v                   |         | V <sub>DD</sub> |
| Input Low Voltage                                    | V <sub>IL</sub>  | 0 (V <sub>SS</sub> )   |         | +0.8v           |
| Supply Current (Logic only, not including backlight) | V <sub>DD</sub> = +5.0v<br>I <sub>DD</sub>                 | 1.5 mA                 |         | 4.0 mA          |

*\*For more information, see [DC Characteristics on page 12 of Appendix D, S6B0108 64 CH Segment Driver for Dot Matrix LCD.](#)*



## INTERFACE PIN FUNCTIONS

| PIN | SIGNAL           | LEVEL    | DIRECTION | DESCRIPTION   |
|-----|------------------|----------|-----------|---|
| 1   | $V_{DD}$         | +5.0v    | –         | Supply voltage for logic  |
| 2   | $V_{SS}$         | 0v       | –         | Ground  |
| 3   | $V_O$            | variable | –         | Supply voltage for driving LCD<br>$V_O = -3.0v$ typical at $V_{DD} = +5v$<br>which gives<br>$V_{LCD} = (V_{DD} - V_O) = 8v$ |
| 4   | DB0              | H/L      | I/O       | Data bit 0  |
| 5   | DB1              | H/L      | I/O       | Data bit 1  |
| 6   | DB2              | H/L      | I/O       | Data bit 2  |
| 7   | DB3              | H/L      | I/O       | Data bit 3  |
| 8   | DB4              | H/L      | I/O       | Data bit 4  |
| 9   | DB5              | H/L      | I/O       | Data bit 5  |
| 10  | DB6              | H/L      | I/O       | Data bit 6  |
| 11  | DB7              | H/L      | I/O       | Data bit 7  |
| 12  | $\overline{CS1}$ | L        | I         | Chip select for controller #1<br>Columns 1 to 64<br>Chip select for controller #2<br>Columns 65 to 128                      |
| 13  | $\overline{CS2}$ | L        | I         | Select Column 65 to Column 128  |
| 14  | $\overline{RST}$ | L        | I         | Controller reset signal   |
| 15  | $R/\overline{W}$ | H/L      |           | Read/write selection input<br>H: read (MPU←module)<br>L: write (MPU→module)   |

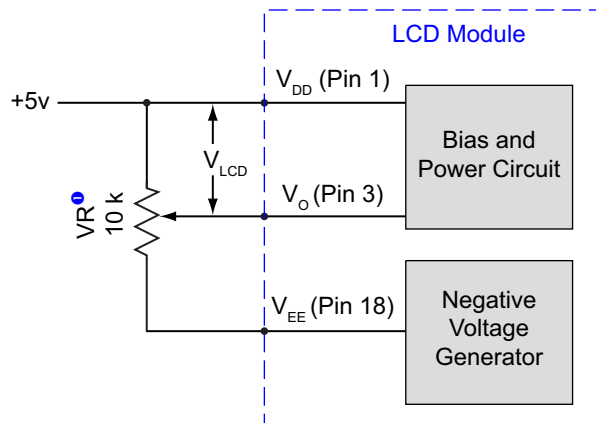


| PIN | SIGNAL          | LEVEL  | DIRECTION | DESCRIPTION   |
|-----|-----------------|--------|-----------|---|
| 16  | D/I             | H/L    | I         | H: Data<br>L: Instruction   |
| 17  | E               | H, H→L | I         | Read/write enable signal<br>H: read data is enabled by a high level<br>H→L: write data is latched on the falling edge |
| 18  | V <sub>EE</sub> | -5v    | O         | Negative voltage output   |
| 19  | A (LED+)        |        |           | Supply voltage for LED<br>"A" (anode) or "+" of LED backlight   |
| 20  | K (LED+)        |        |           | Supply voltage for LED<br>"K" (cathode or kathode for German and original Greek spelling) or "-" of LED backlight     |

For Backlight connections, please refer to [LED BACKLIGHT \(Pg. 15\)](#).

## TYPICAL V<sub>O</sub> CONNECTIONS FOR DISPLAY CONTRAST

Adjust V<sub>O</sub> to -3.0v (V<sub>LCD</sub> = 8.0v) as an initial setting. When the module is operational, readjust V<sub>O</sub> for optimal display appearance.



• Use external control to adjust for optimal display appearance.

Figure 4. Typical V<sub>O</sub> Connections for Display Contrast

## SAMSUNG S6B0107/S6B0108 CONTROLLERS (FORMERLY KS0107B/ KS0108B)

The CFAG12864B-TMI-V uses two Samsung controllers: S6B0107 64 channel common driver and a S6B0108 64 channel segment driver. The previous part number for the Samsung S6B0107 driver was "KS0107B". The previous part number for the Samsung S6B0108 driver was "KS6B108".



For your reference, the most recent versions (July 2001) of the Samsung driver specifications are included as appendixes in this Data Sheet: Samsung S6B0107 64CH Common Driver for Dot Matrix LCD and S6B0108 64CH Segment Driver For Dot Matrix LCD.

Here are links to some of the commonly used sections:

- For DC characteristics, see [page 12 of Appendix D, "DC Characteristics"](#).
- For functional description, see [page 17 of Appendix C, "Functional Description"](#).
- For MPU interface timing characteristics (read and write), see [page 15 of Appendix D, "MPU Interface"](#).
- For display control instruction, see [page 21 of Appendix D, "Display Control Instruction"](#).

## OPTICAL SPECIFICATIONS

| ITEM   | SYMBOL       | CONDITION   | MINIMUM | TYPICAL | MAXIMUM |
|--|--------------|-------------|---------|---------|---------|
| View Angle<br>(Vertical, Horizontal)   | (V) $\theta$ | CR $\geq$ 2 | 20°     |         | 40°     |
|  | (H) $\phi$   | CR $\geq$ 2 | -30°    |         | +30°    |
| Contrast Ratio   | CR           |             |         | 3       |         |
| LCD Response<br>Time*  | T rise       | Ta = 25°C   |         | 200 ms  | 300 ms  |
|  | T fall       | Ta = 25°C   |         | 200 ms  | 300 ms  |
| *Response Time: The amount of time it takes a liquid crystal cell to go from active to inactive or back again. |              |             |         |         |         |

## TEST CONDITIONS AND DEFINITIONS FOR OPTICAL CHARACTERISTICS

### Test Conditions

- Operating Voltage (V<sub>LCD</sub>): V<sub>OP</sub>
- Viewing Angle
  - Vertical (V) $\theta$ : 0°
  - Horizontal (H) $\phi$ : 0°
- Frame Frequency: 64 Hz (nominal)
- Driving Waveform: 1/64 Duty, 1/9 Bias
- Ambient Temperature (Ta): 25°C



### Definition Operation Voltage ( $V_{op}$ )

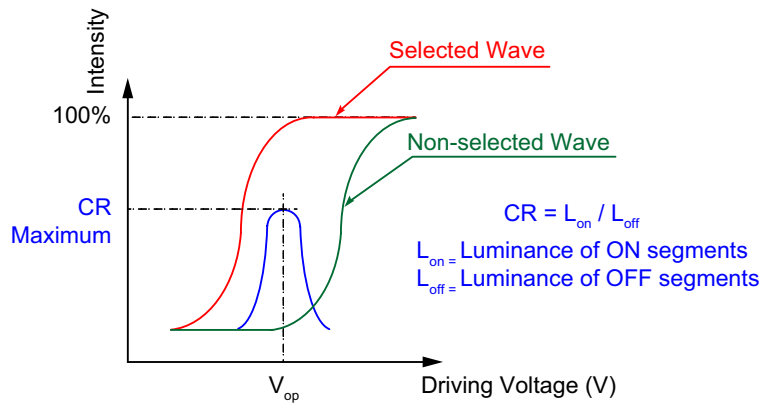


Figure 5. Definition of Operation Voltage ( $V_{OP}$ )

### Definition of Response Time ( $Tr$ , $Tf$ )

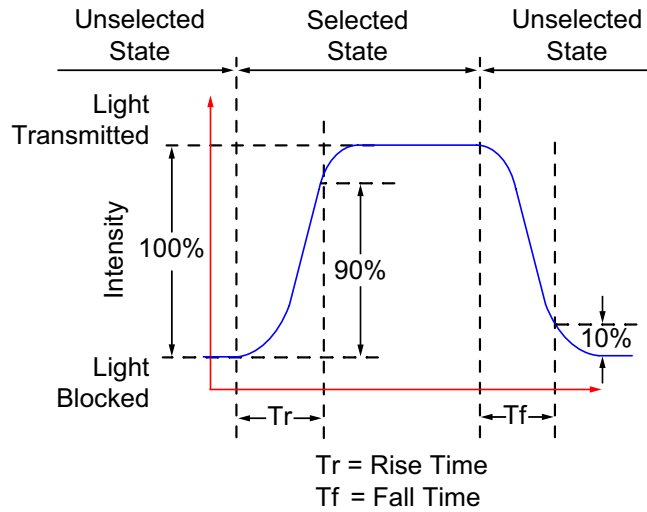


Figure 6. Definition of Response Time ( $Tr$ ,  $Tf$ )



### Definition of Vertical and Horizontal Viewing Angles (CR>2)

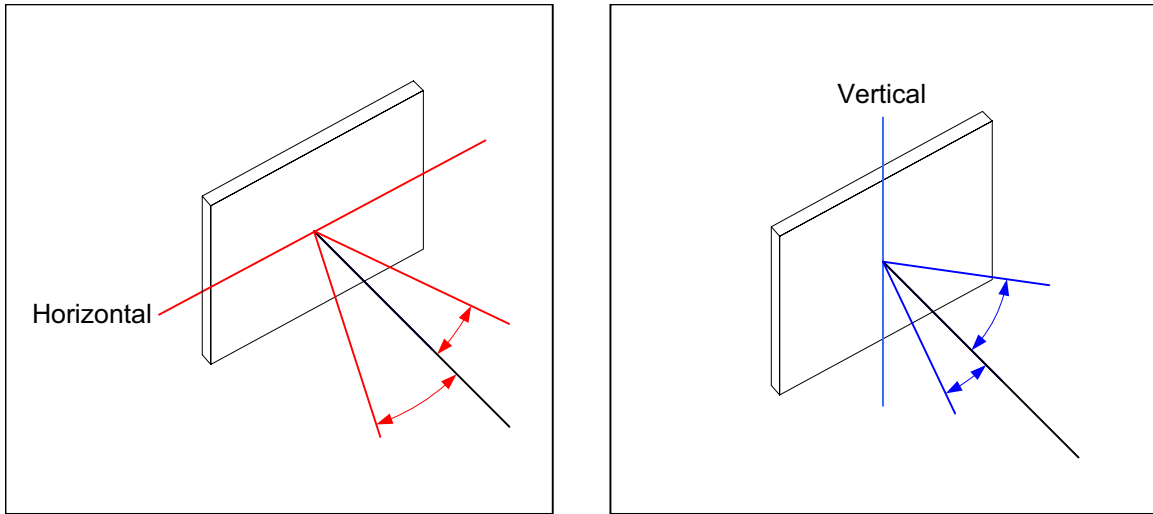


Figure 7. Definition of Horizontal and Vertical Viewing Angles (CR>2)

### Definition of 6 O’Clock and 12:00 O’Clock Viewing Angles

A 6:00 o’clock viewing angle is a bottom viewing angle like what you would see when looking at a cell phone or calculator. A 12:00 o’clock viewing angle is a top viewing angle like what you would see when looking at the gauges in a golf cart or airplane.

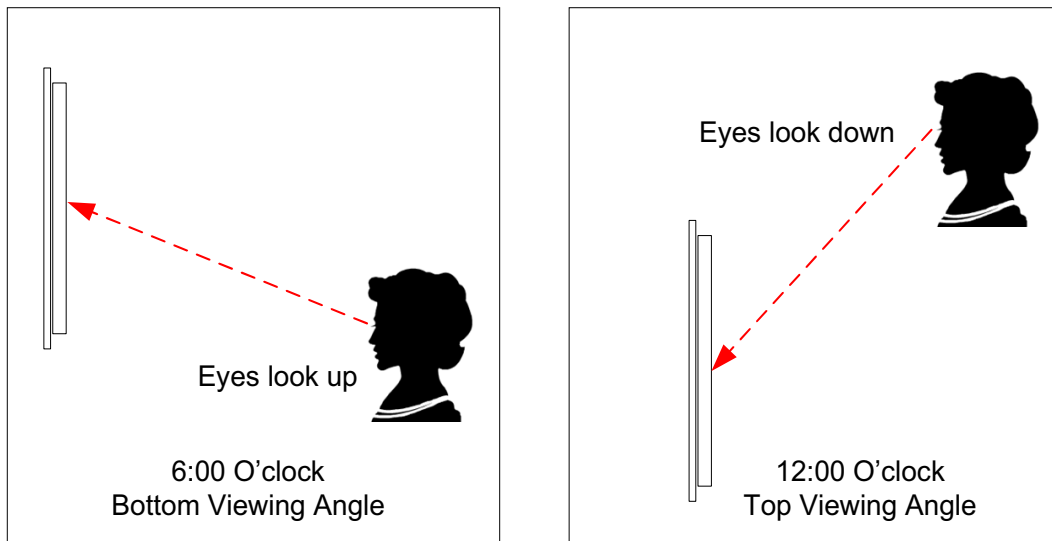


Figure 8. 6:00 O’Clock and 12:00 O’Clock Viewing Angles

## LED BACKLIGHT

You can connect the CFAG12864B-TMI-V backlight by one of these two methods:

- Solder leads from your PCB’s circuit to the “A” and “K” connectors on the right edge of the display (glass facing up).
- Make connections to your PCB using Pins 19 (A (LED+)) and 20 (K (LED+)) on the display module’s connector.



| <b>LED Backlight Characteristics</b><br><i>Illuminated light dots on blue background</i> |                       |                       |         |
|--|-----------------------|-----------------------|---------|
| PARAMETER  | MINIMUM               | TYPICAL               | MAXIMUM |
| Forward Current ( $I_{LED}$ )<br>$V = +3.5v$   | 48 mA                 | 60 mA                 | 90 mA*  |
| Forward Voltage ( $V_{LED}$ )  | +3.4v                 | +3.5v                 | +3.6v   |
| Reverse Voltage ( $V_R$ )  |                       | +5v                   |         |
| Luminous Intensity**<br>(IV)<br>$I_{LED} = 60\text{ mA}$                                 | 150 cd/m <sup>2</sup> | 190 cd/m <sup>2</sup> |         |
| Chromaticity   | x                     | 0.275                 | 0.290   |
|  | y                     | 0.300                 | 0.315   |

\*Driving the backlight above 60 mA will shorten its lifetime.  
 \*\*Direct measurement of backlight—the backlight is not measured through the LCD.

The CFAG12864B-TMI-V backlight uses LEDs. The backlight is easy to use properly but it is also easily damaged by abuse.

**NOTE**  
 Do not connect +5v directly to the backlight terminals. This will ruin the backlight.

**NOTE**  
 We recommend that the white LED backlight be dimmed or turned off during periods of inactivity to conserve the LEDs' lifetime.

LEDs are "current" devices. The brightness is controlled by the current flowing through it, not the voltage across it. Ideally, a current source would be used to drive the LEDs. In practice, a simple current limiting resistor will work well in most applications and is much less complex than a current source.

You need to know what the supply (forward) voltage of the LEDs will be so you can calculate a current limiting resistor ( $R_{LIMIT}$ ). The forward voltage will vary slightly from display to display.

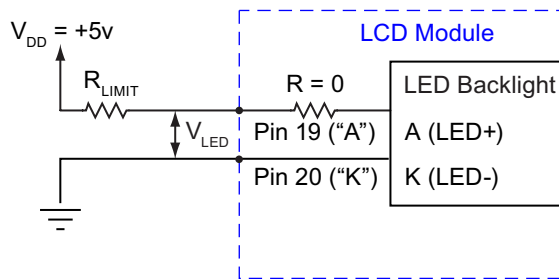


Figure 9. LED Backlight Connection Using Pin 19 and Pin 20





The general equation to calculate  $R_{LIMIT}$  is:

$$R_{LIMIT} \text{ (minimum)} = \frac{V_{DD} \text{ (supply voltage)} - V_{LED} \text{ (LED forward voltage)}}{I_{LED} \text{ (maximum LED current)}}$$

The specific  $R_{LIMIT}$  calculation for the CFAG12864B-TMI-V at  $V_{DD} = +5v$  is:

$$R_{LIMIT} = \frac{5v - 3.5v}{0.06 \text{ A (maximum)}} = 25\Omega \text{ (minimum)}$$

The backlight may be dimmed by PWM (Pulse Width Modulation). The typical range for the PWM frequency is from 100 to 300 Hz.

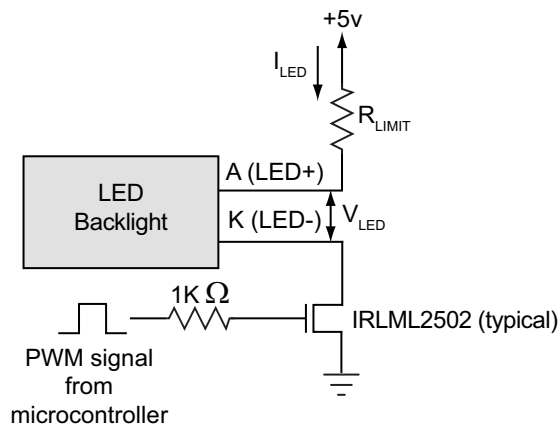


Figure 10. Typical LED Backlight Connections for PWM Dimming

## PRODUCT RELIABILITY

| ITEM  | SPECIFICATION                     |                         |
|---|-----------------------------------|-------------------------|
| Module, excluding backlight.  | 50,000 to 100,000 hours (typical) |                         |
| White LED Backlight ( $I_{LED} < 60 \text{ mA}$ )*<br>* We recommend that the backlight of the white LED backlit modules be dimmed or turned off during periods of inactivity to conserve the white LED backlight lifetime. | Power-On Hours                    | % of Initial Brightness |
|   | <10,000                           | >90%                    |
|   | <50,000                           | >50%                    |



## CARE AND HANDLING PRECAUTIONS

---

For optimum operation of the module and to prolong its life, please follow the precautions described below.

### ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard anti-static precautions as you would for any other PCB such as expansion cards or motherboards.

### DESIGN AND MOUNTING

- The exposed surface of the LCD “glass” is actually a polarizer laminated on top of the glass. To protect the polarizer from damage, the CFAG12864B-TMI-V ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of a soft plastic and is easily scratched or damaged. To protect the polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the CFAG12864B-TMI-V, leaving a small gap between the plate and the display surface. We recommend GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- Do not modify the mounting tab of the metal bezel or make connections to it.
- Solder only to the I/O terminals. Use care when removing solder—it is possible to damage the PCB.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.

### AVOID SHOCK, IMPACT, TORQUE, AND TENSION

- Do not expose the module to strong mechanical shock, impact, torque, and tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

### IF LCD PANEL BREAKS

- If the LCD panel breaks, be careful to not get the liquid crystal fluid in your mouth or eyes.
- If the liquid crystal fluid touches your skin, clothes, or work surface, wash it off immediately using soap and plenty of water.
- Do not eat the LCD panel.

### CLEANING

- The polarizer (laminated to the glass) is made out of a soft plastic and is easily scratched or damaged. Be very careful when you clean the polarizer. Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter.
- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips). Damage will be especially obvious on “negative” modules (module that appear dark when “off”).



## OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product". This module is not "user friendly" and connecting them to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at <http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257>.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: a minimum of -20°C to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
  - At lower temperatures of this range, response time is delayed.
  - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Adjust backlight brightness so the display is readable but not too bright. Dim or turn off the backlight during periods of inactivity to conserve the white LED backlight lifetime.
- Operate away from dust, moisture, and direct sunlight.

## STORAGE

- Store in an ESD-approved container away from dust, moisture, and direct sunlight.
- Observe the storage temperature limitations: a minimum of -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.



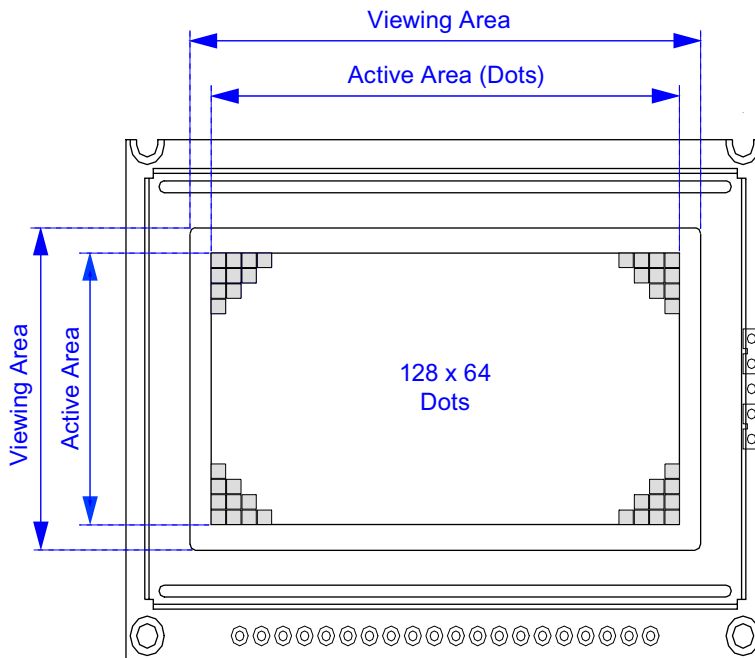
# APPENDIX A: QUALITY ASSURANCE STANDARDS

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## INSPECTION CONDITIONS

- Environment
  - Temperature:  $25\pm 5^{\circ}\text{C}$
  - Humidity: 30~85% RH
- For visual inspection of active display area
  - Source lighting: two 20 Watt or one 40 Watt fluorescent light
  - Display adjusted for best contrast
  - Viewing distance:  $30\pm 5$  cm (about 12 inches)
  - Viewable angle: inspect at  $45^{\circ}$  angle of vertical line right and left, top and bottom

## DEFINITION OF ACTIVE AREA AND VIEWING AREA





## ACCEPTANCE SAMPLING

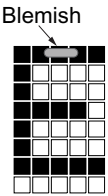
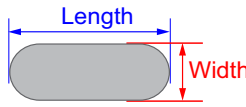
| DEFECT TYPE   | AQL*  |
|---|-------|
| Major   | ≤.65% |
| Minor   | <1.0% |
| * Acceptable Quality Level: maximum allowable error rate or variation from standard |       |

## DEFECTS CLASSIFICATION

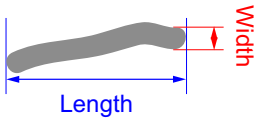
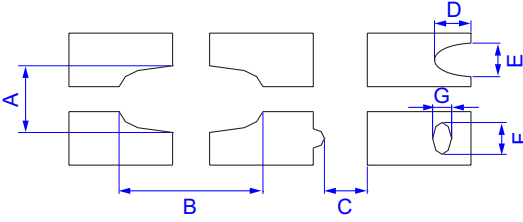
Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

## ACCEPTANCE STANDARDS

| # | DEFECT TYPE   | CRITERIA  |                                       | MAJOR / MINOR         |       |
|---|---|---|---------------------------------------|-----------------------|-------|
| 1 | Electrical defects                                      | 1. No display, display malfunctions, or shorted segments.<br>2. Current consumption exceeds specifications.                 |                                       | Major                 |       |
| 2 | Viewing area defect                                     | Viewing area does not meet specifications. (See <a href="#">Inspection Conditions (Pg. 20)</a> .)                           |                                       | Major                 |       |
| 3 | Contrast adjustment defect                              | Contrast adjustment fails or malfunctions.  |                                       | Major                 |       |
| 4 | Blemishes or foreign matter on display segments         |    | <i>Defect Size</i>                    | <i>Acceptable Qty</i> | Minor |
|   |   |   | ≤0.3 mm                               | 3                     |       |
|   |   |   | ≤2 defects within 10 mm of each other |                       |       |
| 5 | Blemishes or foreign matter outside of display segments | Defect Size = (Width + Length)/2<br><br> | <i>Defect Size</i>                    | <i>Acceptable Qty</i> | Minor |
|   |   |   | ≤0.15 mm                              | Ignore                |       |
|   |   |   | 0.15 to 0.20 mm                       | 3                     |       |
|   |   |   | 0.20 to 0.25 mm                       | 2                     |       |
|   |   |   | 0.25 to 0.30 mm                       | 1                     |       |



| #  | DEFECT TYPE  | CRITERIA  |   |                       | MAJOR / MINOR |
|----|--|---|---|-----------------------|---------------|
| 6  | Dark lines or scratches in display area<br><br> | <i>Defect Width</i>   | <i>Defect Length</i>                      | <i>Acceptable Qty</i> | Minor         |
|    |  | ≤0.03 mm  | ≤3.0 mm                                   | 3                     |               |
|    |  | 0.03 to 0.05  | ≤2.0 mm                                   | 2                     |               |
|    |  | 0.05 to 0.08  | ≤2.0 mm                                   | 1                     |               |
|    |  | 0.08 to 0.10  | ≤3.0 mm                                   | 0                     |               |
|    |  | ≥0.10   | >3.0 mm                                   | 0                     |               |
| 7  | Bubbles between polarizer film and glass   | <i>Defect Size</i>  | <i>Acceptable Qty</i>                     | Minor                 |               |
|    |  | ≤2.0 mm   | Ignore                                    |                       |               |
|    |  | 0.20 to 0.40 mm   | 3   |                       |               |
|    |  | 0.40 to 0.60 mm   | 2   |                       |               |
|    |  | ≥0.60 mm  | 0   |                       |               |
| 8  | Display pattern defect<br><br>                | <i>Dot Size</i>   | <i>Acceptable Qty</i>                     | Minor                 |               |
|    |  | $((A+B)/2) \leq 0.2$ mm   | ≤3 total defects<br>≤2 pinholes per digit |                       |               |
|    |  | C > 0 mm  |   |                       |               |
|    |  | $((D+E)/2) \leq 0.25$ mm  |   |                       |               |
|    |  | $((F+G)/2) \leq 0.25$ mm  |   |                       |               |
|    |  |   |   |                       |               |
| 9  | Backlight defects  | 1. Light fails or flickers. (Major)<br>2. Color and luminance do not correspond to specifications. (Major)<br>3. Exceeds standards for display's blemishes or foreign matter ( <a href="#">see test 5, Pg. 21</a> ), and dark lines or scratches ( <a href="#">see test 6, Pg. 22</a> ). (Minor)                          |   |                       | See list<br>← |
| 10 | PCB defects  | 1. Oxidation or contamination on connectors.*<br>2. Wrong parts, missing parts, or parts not in specification.*<br>3. Jumpers set incorrectly. (Minor)<br>4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth. (Minor)<br>*Minor if display functions correctly. Major if the display fails. |   |                       | See list<br>← |



| #  | DEFECT TYPE       | CRITERIA   | MAJOR / MINOR |
|----|-------------------|--|---------------|
| 11 | Soldering defects | 1. Unmelted solder paste.<br>2. Cold solder joints, missing solder connections, or oxidation.*<br>3. Solder bridges causing short circuits.*<br>4. Residue or solder balls.<br>5. Solder flux is black or brown.<br>*Minor if display functions correctly. Major if the display fails. | Minor         |



## APPENDIX B: SAMPLE CODE

---

### SOURCES FOR DRIVER LIBRARIES

Graphic LCD driver libraries may save you a lot of time and help you develop a more professional product. Two library sources are [RAMTEX](#) and [easyGUI](#).

### C++ INITIALIZATION EXAMPLE

*Below is an example of an initialization sequence based on Atmel's ATmega32.*

```
//=====
// LOW_LCD.C: Low-level lcd display routines.
// Samsung KS0107+KS0108 (S6B0107+S6B0108) LCD Controller
// Atmel ATmega32 processor @ 16MHz
// WinAVR / AVR GCC + Atmel AVR Studio
// Written by Brent A. Crosby
// Copyright 2005, CrystalFontz America, Inc. http://www.crystalfontz.com
//=====
#include <avr/io.h>
#include <avr/iom32.h>
#include <string.h>
#include <avr/delay_x.h>
#include "typedefs.h"
#include "utils.h"
#include "low_lcd.h"
//=====
//This is the display memory.
ubyte
    display[8][128]; //1024 bytes
//=====
void write_both_lcd_control_registers(ubyte data)
{
    //We need to wait until both controller's busy bits are clear.
    //Talk to the status (instruction) register.
    //(Must happen 140nS before the RISING edge of E.)
    PORTC&=~PORTC1_LCD_DI;
    //Tell the LCD we are going to be reading it
    //(Must happen 140nS before the RISING edge of E.)
    PORTC|=PORTC6_LCD_RW;
    //Talk to the left controller only
    //(Must happen 140nS before the RISING edge of E.)
    PORTC&=~PORTC0_LCD_CS1;
    PORTD|=PORTD6_LCD_CS2;
    //Make port A high-impedance
    DDRA=0x00;
    //Enable the selected controller's read data onto the port
    PORTC|=PORTC7_LCD_E;
    //The data is not valid for 320nS
    _delay_cycles(4); //375nS
}
```





```
//Wait for the busy bit to drop
while(PINA&0x80);
//Terminate the read
PORTC&=~PORTC7_LCD_E;

//Talk to the right controller only
PORTC|=PORTC0_LCD_CS1; //125nS
PORTD&=~PORTD6_LCD_CS2; //125nS
//(Must happen 140nS before the RISING edge of E.)
//(E LOW pulse must be 450mS min)
_delay_cycles(2); //250nS

//Enable the selected controller's read data onto the port
PORTC|=PORTC7_LCD_E;
//The data is not valid for 320nS
_delay_cycles(4);
//Wait for the busy bit to drop
while(PINA&0x80);
//Terminate the read
PORTC&=~PORTC7_LCD_E;

//Tell the LCD that we are writing to it.
//(Must happen 140nS before the RISING edge of E.)
PORTC&=~PORTC6_LCD_RW; //125nS
//Talk to both controllers
//(Must happen 140nS before the RISING edge of E.)
PORTC&=~PORTC0_LCD_CS1; //125nS
//stretch LOW E pulse width above the minimum of 450nS
_delay_cycles(2); //250nS
//Strobe the E pin. We are still aimed at the status/instruction register.
PORTC|=PORTC7_LCD_E;
//Write the data to the output latches of port A
//(Must happen 200nS before the FALLING edge of E.)
PORTA=data; //62.5nS
//Go back to port A as an output
DDRA=0xFF; //125nS
//stretch HIGH E pulse width above the minimum of 450nS
_delay_cycles(3); //312.5nS
PORTC&=~PORTC7_LCD_E;
}
//=====
// PORTC0_LCD_CS1 and PORTD6_LCD_CS2 must be set to select the desired
// controller
//-----
void write_lcd_data(ubyte data)
{
//We need to wait until the busy bit is clear.
//Talk to the status (instruction) register.
//(Must happen 140nS before the RISING edge of E.)
PORTC&=~PORTC1_LCD_DI;
//Tell the LCD we are going to be reading it
//(Must happen 140nS before the RISING edge of E.)
PORTC|=PORTC6_LCD_RW;
//Make port A high-impedance
```



```
DDRA=0x00;
//Enable the selected controller's read data onto the port
PORTC|=PORTC7_LCD_E;
//The data from the LCD is not valid for 320nS
_delay_cycles(4); //375nS
//Wait for the busy bit to drop
while(PINA&0x80);
//Terminate the read
PORTC&=~PORTC7_LCD_E;
//Tell the LCD that we are writing to it.
//(Must happen 140nS before the RISING edge of E.)
PORTC&=~PORTC6_LCD_RW; //125nS
//Aim at the data register.
//(Must happen 140nS before the RISING edge of E.)
PORTC|=PORTC1_LCD_DI; //125nS
//stretch LOW E pulse width above the minimum of 450nS
_delay_cycles(2); //250nS
//Strobe the E pin.
PORTC|=PORTC7_LCD_E;
//Write the data to the output latches of port A
//(Must happen 200nS before the FALLING edge of E.)
PORTA=data; //62.5nS
//Go back to port A as an output
DDRA=0xFF; //125nS
//stretch HIGH E pulse width above the minimum of 450nS
_delay_cycles(3); //312.5nS
//Terminate the write
PORTC&=~PORTC7_LCD_E;
}
//=====
// Takes about 5.08ms (201.7KB/S) reading busy flag
void UpdateLCD(void)
{
register ubyte
 *left_data;
register ubyte
 *right_data;
register ubyte
 page_address;
register ubyte
 column_address;

//Initialize our source data pointers.
left_data=&display[0][0];
right_data=&display[0][64];

//Make sure we are not in a write cycle
PORTC&=~PORTC7_LCD_E;

//Make sure the LCD thinks we are writing
PORTC&=~PORTC6_LCD_RW;

for(page_address=0;page_address<=7;page_address++)
{
```



```
//Set Y address (page, or horizontal stripe of 8 pixels) (controller docs call this
"X")
write_both_lcd_control_registers(0xB8|page_address);
//Set X address 0 (right to left) (controller docs call this "Y")
write_both_lcd_control_registers(0x40);

for(column_address=0;column_address<=63;column_address++)
{
//Talk to the left controller only
PORTC&=~PORTC0_LCD_CS1;
PORTD|=PORTD6_LCD_CS2;
write_lcd_data(*left_data++);
//Talk to the right controller only
PORTC|=PORTC0_LCD_CS1;
PORTD&=~PORTD6_LCD_CS2;
write_lcd_data(*right_data++);
}
//Skip down to the next line
left_data+=64;
right_data+=64;
}
}
//=====
void InitializeLCD(void)
{
//Display on
write_both_lcd_control_registers(0x3F);

//Set Start Line 0
write_both_lcd_control_registers(0xC0);

//Clear the display memory
memset(display,0x00,sizeof(display));
}
//=====
```



## APPENDIX C: SAMSUNG S6B0107 64 CH COMMON DRIVER

---

The complete Samsung's *S6B0107 64 CH Common Driver for Dot Matrix LCD* specifications follows.

# S6B0107

## 64CH COMMON DRIVER FOR DOT MATRIX LCD

July 2001

Ver. 0.0

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### **Precautions for Light**

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

| <b>S6B0107 Specification Revision History</b> |                |             |
|---|----------------|-------------|
| <b>Version</b>                                | <b>Content</b> | <b>Date</b> |
| 0.0   | Original       | July.2001   |

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## INTRODUCTION

The S6B0107 (TQFP type: S6B2107) is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 output drivers. It generates the timing signal to control the S6B0108 (64 channel segment driver - TQFP type: S6B2108). The S6B0107 is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the S6B0108 (64 channel segment driver).

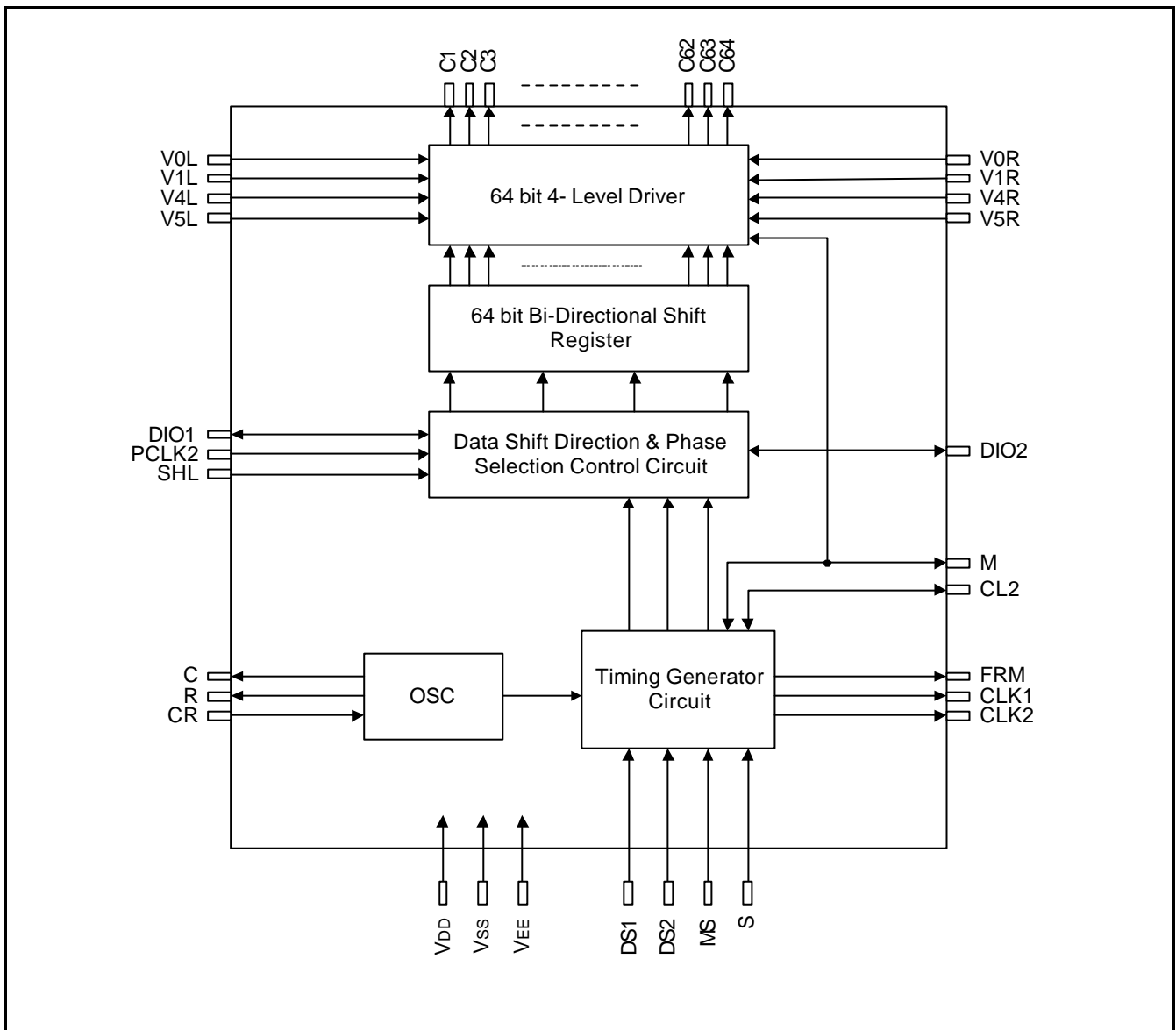
## FEATURES

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage: + 5V  $\pm$  10%
- LCD driving voltage: 8V - 17V ( $V_{DD}-V_{EE}$ )
- Interface

| Driver        |         | Controller |
|---------------|---------|------------|
| COMMON        | SEGMENT |            |
| Other S6B0107 | S6B0108 | MPU        |

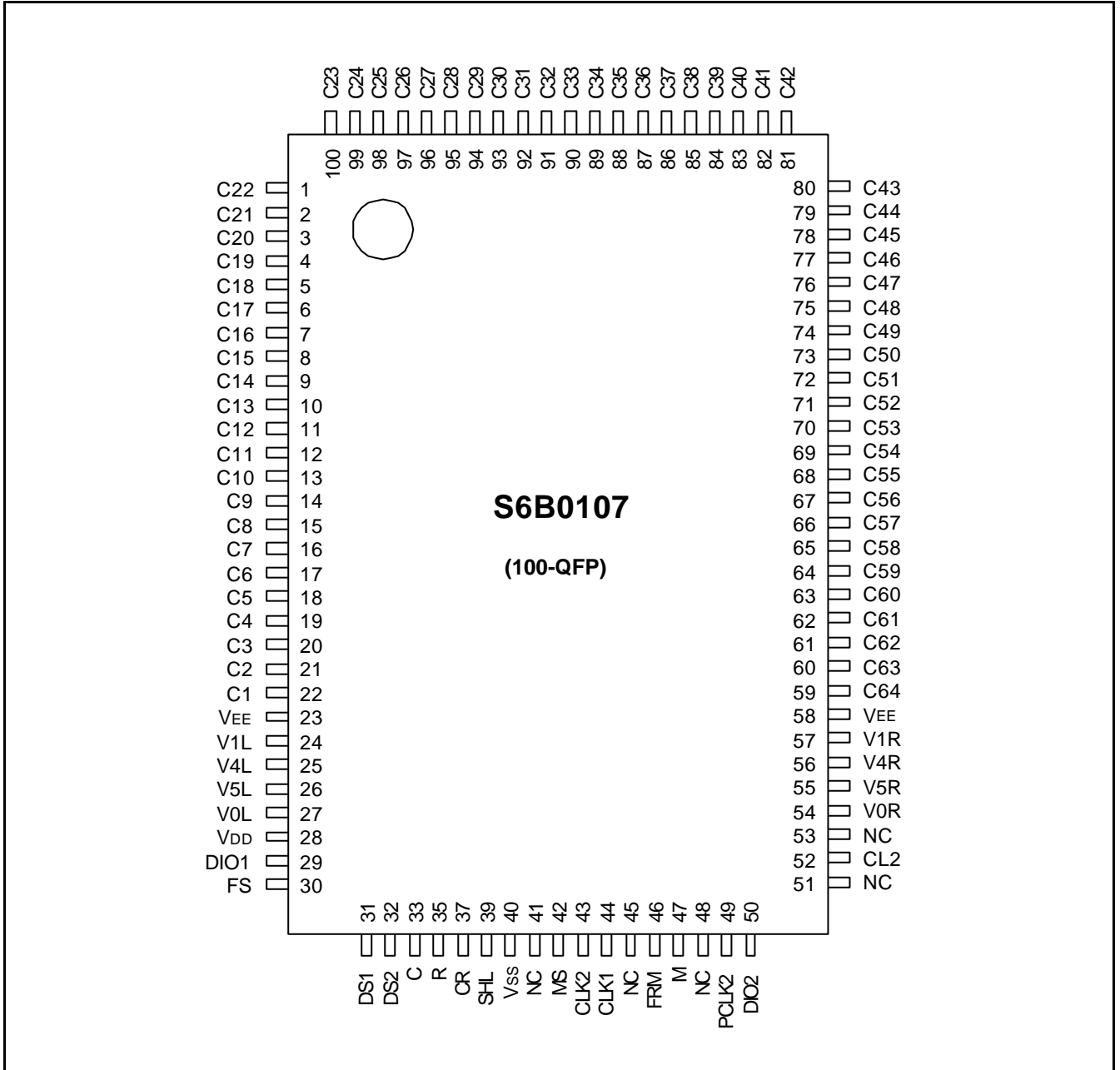
- High voltage CMOS process
- 100QFP/100TQFP and bare chip available

**BLOCK DIAGRAM**

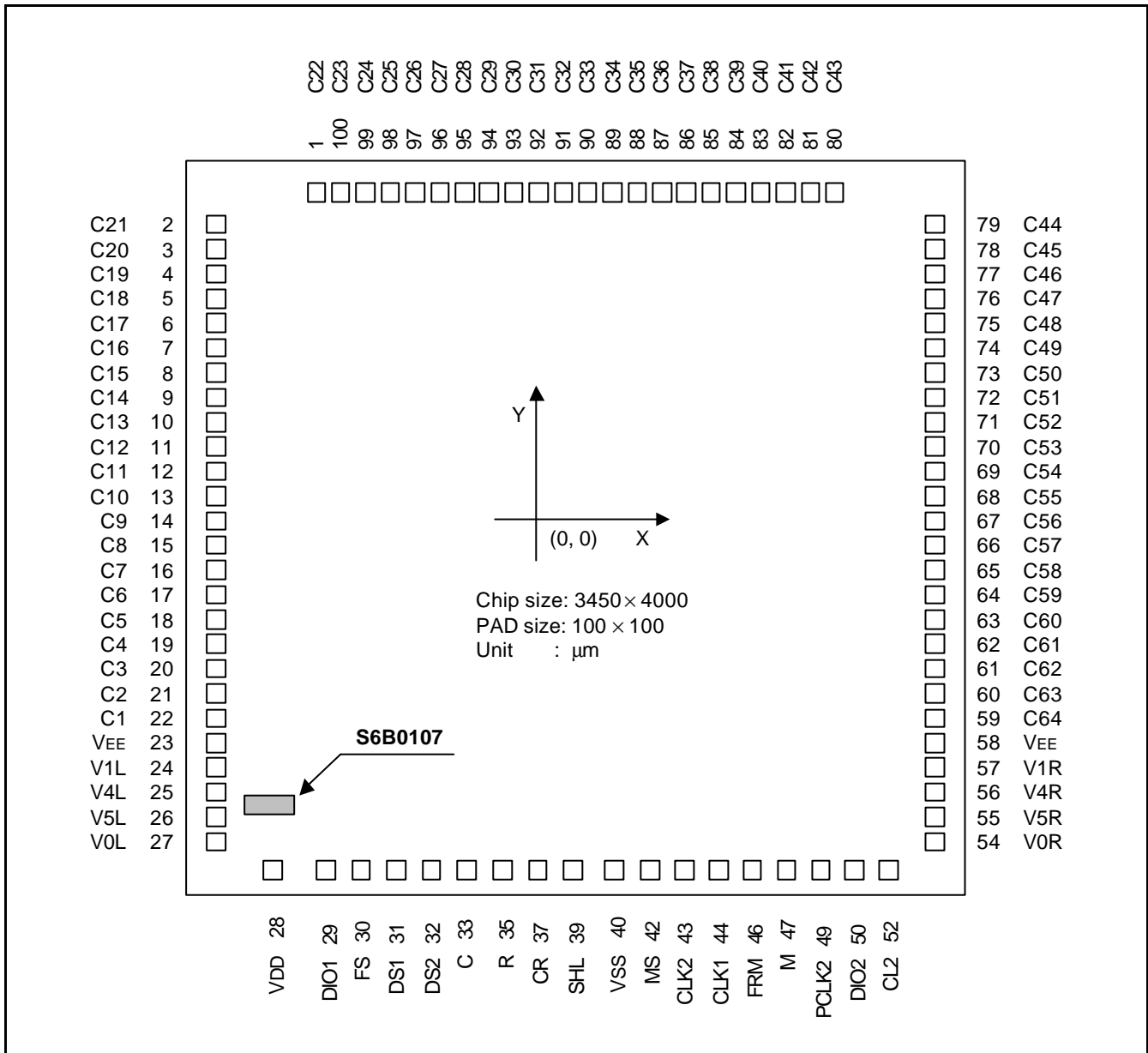


**PIN CONFIGURATION**

**100-QFP**



PAD DIAGRAM (CHIP LAYOUT FOR THE 100QFP)

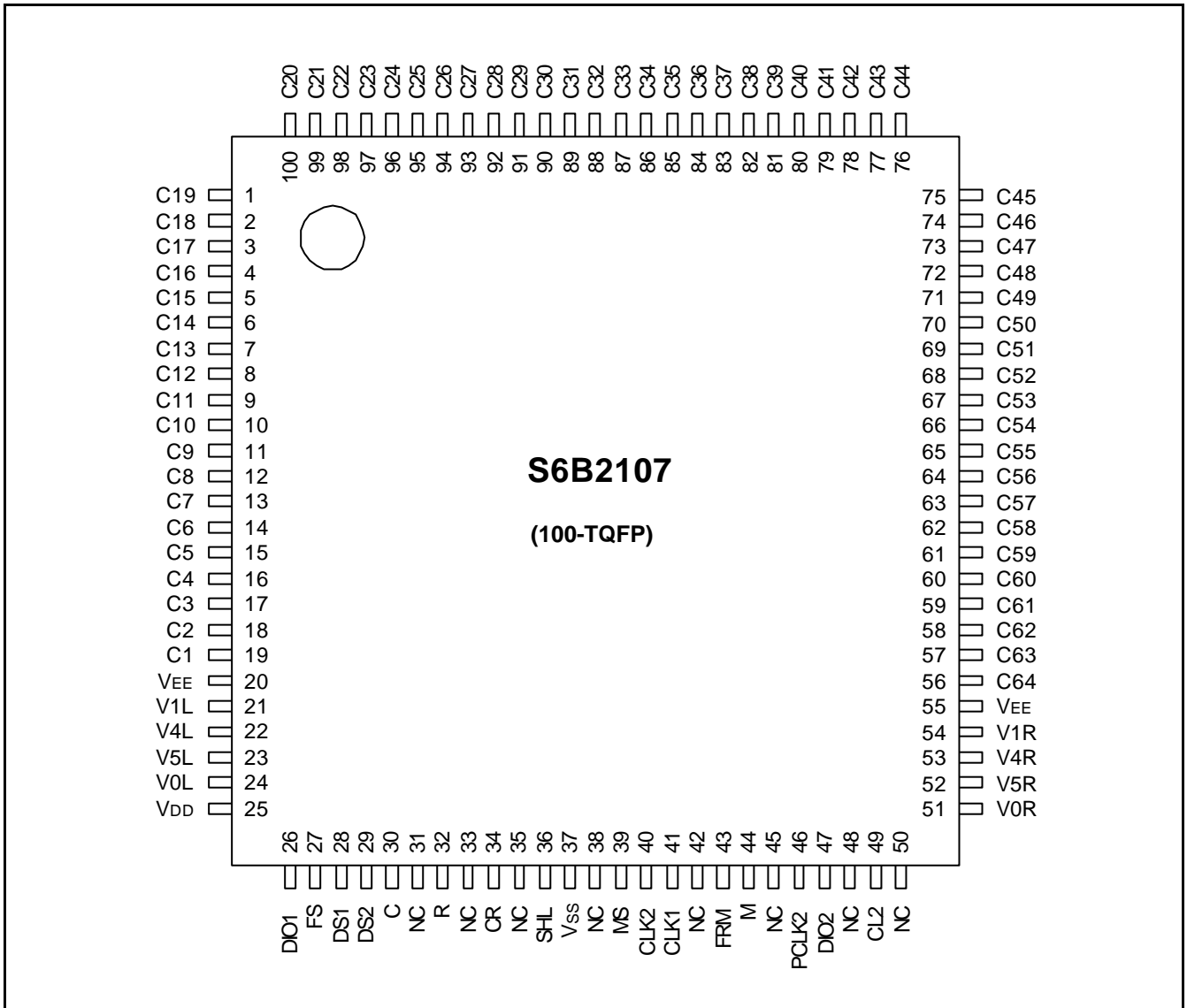


There is the mark S6B0107 on the center of the chip.

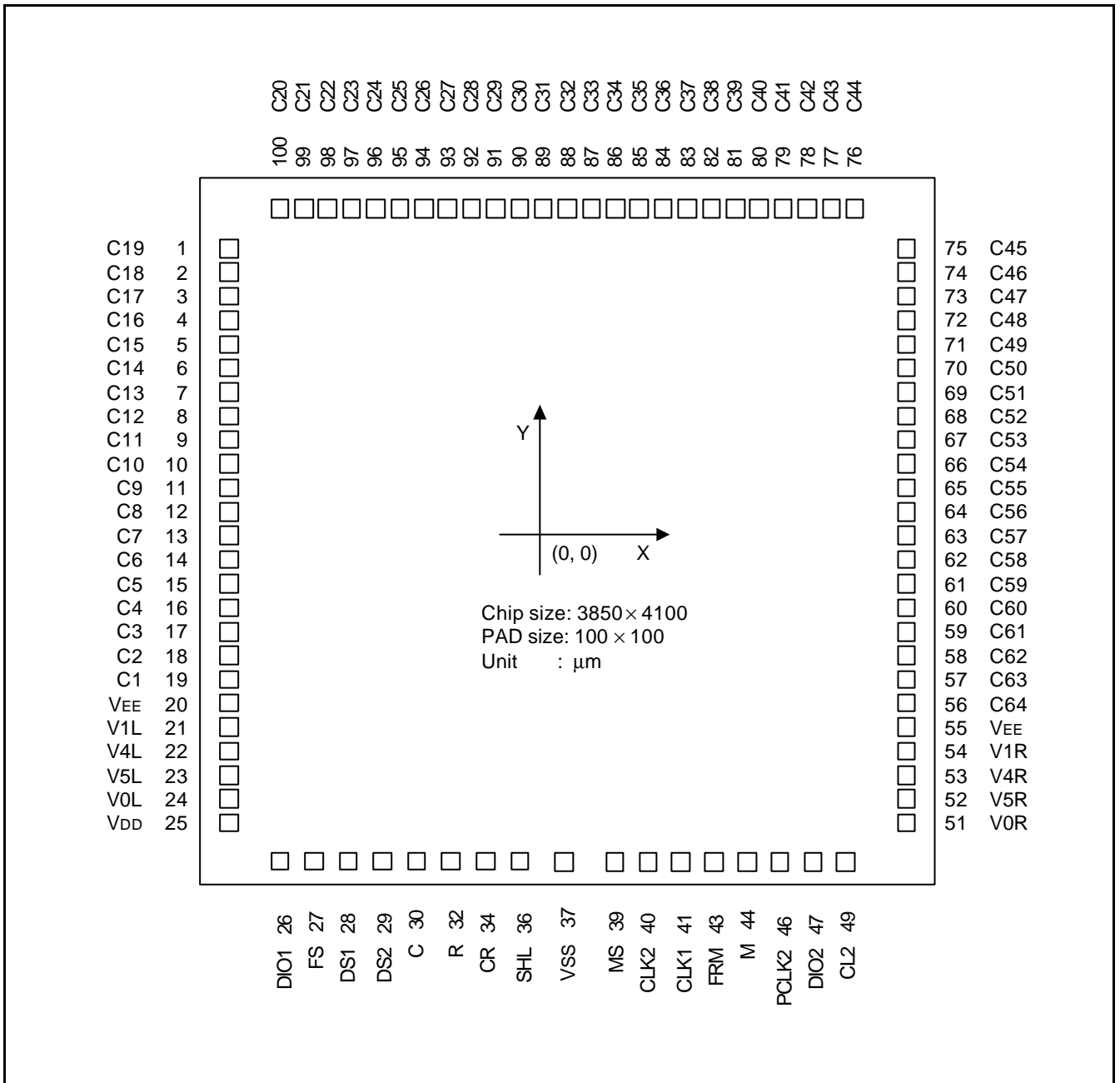
## PAD CENTER COORDINATES (100QFP)

| Pad Number | Pad Name        | Coordinate |        | Pad Number | Pad Name        | Coordinate |       | Pad Number | Pad Name | Coordinate |        |
|------------|-----------------|------------|--------|------------|-----------------|------------|-------|------------|----------|------------|--------|
|            |                 | X          | Y      |            |                 | X          | Y     |            |          | X          | Y      |
| 1          | C22             | -1314.5    | 1775.4 | 32         | DS2             | -677.6     | -1775 | 71         | C52      | 1500.9     | 630    |
| 2          | C21             | -1499.9    | 1630   | 33         | C               | -527.6     | -1775 | 72         | C51      | 1500.9     | 755    |
| 3          | C20             | -1499.9    | 1505   | 35         | R               | -377.6     | -1775 | 73         | C50      | 1500.9     | 880    |
| 4          | C19             | -1499.9    | 1380   | 37         | CR              | -227.6     | -1775 | 74         | C49      | 1500.9     | 1005   |
| 5          | C18             | -1499.9    | 1255   | 39         | SHL             | -77.6      | -1775 | 75         | C48      | 1500.9     | 1130   |
| 6          | C17             | -1499.9    | 1130   | 40         | V <sub>SS</sub> | 113.8      | -1775 | 76         | C47      | 1500.9     | 1255   |
| 7          | C16             | -1499.9    | 1005   | 42         | MS              | 308.7      | -1775 | 77         | C46      | 1500.9     | 1380   |
| 8          | C15             | -1499.9    | 880    | 43         | CLK2            | 458.7      | -1775 | 78         | C45      | 1500.9     | 1505   |
| 9          | C14             | -1499.9    | 755    | 44         | CLK1            | 608.7      | -1775 | 79         | C44      | 1500.9     | 1630   |
| 10         | C13             | -1499.9    | 630    | 46         | FRM             | 758.7      | -1775 | 80         | C43      | 1310.5     | 1775.4 |
| 11         | C12             | -1499.9    | 505    | 47         | M               | 908.7      | -1775 | 81         | C42      | 1185.5     | 1775.4 |
| 12         | C11             | -1499.9    | 380    | 49         | PCLK2           | 1058.7     | -1775 | 82         | C41      | 1060.5     | 1775.4 |
| 13         | C10             | -1499.9    | 255    | 50         | DI02            | 1208.7     | -1775 | 83         | C40      | 935.5      | 1775.4 |
| 14         | C9              | -1499.9    | 130    | 52         | CL2             | 1358.7     | -1775 | 84         | C39      | 810.5      | 1775.4 |
| 15         | C8              | -1499.9    | 5      | 54         | V0R             | 1500.9     | -1495 | 85         | C38      | 685.5      | 1775.4 |
| 16         | C7              | -1499.9    | -120   | 55         | V5R             | 1500.9     | -1370 | 86         | C37      | 560.5      | 1775.4 |
| 17         | C6              | -1499.9    | -245   | 56         | V4R             | 1500.9     | -1245 | 87         | C36      | 435.5      | 1775.4 |
| 18         | C5              | -1499.9    | -370   | 57         | V1R             | 1500.9     | -1120 | 88         | C35      | 310.5      | 1775.4 |
| 19         | C4              | -1499.9    | -495   | 58         | V <sub>EE</sub> | 1500.9     | -995  | 89         | C34      | 185.5      | 1775.4 |
| 20         | C3              | -1499.9    | -620   | 59         | C64             | 1500.9     | -870  | 90         | C33      | 60.5       | 1775.4 |
| 21         | C2              | -1499.9    | -745   | 60         | C63             | 1500.9     | -745  | 91         | C32      | -64.5      | 1775.4 |
| 22         | C1              | -1499.9    | -870   | 61         | C62             | 1500.9     | -620  | 92         | C31      | -189.5     | 1775.4 |
| 23         | V <sub>EE</sub> | -1499.9    | -995   | 62         | C61             | 1500.9     | -495  | 93         | C30      | -314.5     | 1775.4 |
| 24         | V1L             | -1499.9    | -1120  | 63         | C60             | 1500.9     | -370  | 94         | C29      | -439.5     | 1775.4 |
| 25         | V4L             | -1499.9    | -1245  | 64         | C59             | 1500.9     | -245  | 95         | C28      | -564.5     | 1775.4 |
| 26         | V5L             | -1499.9    | -1370  | 65         | C58             | 1500.9     | -120  | 96         | C27      | -689.5     | 1775.4 |
| 27         | V0L             | -1499.9    | -1495  | 66         | C57             | 1500.9     | 5     | 97         | C26      | -814.5     | 1775.4 |
| 28         | V <sub>DD</sub> | -1345.6    | -1775  | 67         | C56             | 1500.9     | 130   | 98         | C25      | -939.5     | 1775.4 |
| 29         | DI01            | -1127.6    | -1775  | 68         | C55             | 1500.9     | 255   | 99         | C24      | -1064.5    | 1775.4 |
| 30         | FS              | -977.6     | -1775  | 69         | C54             | 1500.9     | 380   | 100        | C23      | -1189.5    | 1775.4 |
| 31         | DS1             | -827.6     | -1775  | 70         | C53             | 1500.9     | 505   |            |          |            |        |

100-TQFP (S6B2107)



PAD DIAGRAM (CHIP LAYOUT FOR THE 100-TQFP)



NOTE: There is the mark S6B2107 on the center of the chip.

## PAD CENTER COORDINATES (100-TQFP)

| Pad Number | Pad Name        | Coordinate |       | Pad Number | Pad Name        | Coordinate |       | Pad Number | Pad Name | Coordinate |      |
|------------|-----------------|------------|-------|------------|-----------------|------------|-------|------------|----------|------------|------|
|            |                 | X          | Y     |            |                 | X          | Y     |            |          | X          | Y    |
| 1          | C19             | -1697      | 1534  | 35         | NC              |            |       | 69         | C51      | 1697       | 784  |
| 2          | C18             | -1697      | 1409  | 36         | SHL             | -195       | -1821 | 70         | C50      | 1697       | 909  |
| 3          | C17             | -1697      | 1284  | 37         | V <sub>SS</sub> | 0          | -1821 | 71         | C49      | 1697       | 1034 |
| 4          | C16             | -1697      | 1159  | 38         | NC              |            |       | 72         | C48      | 1697       | 1159 |
| 5          | C15             | -1697      | 1034  | 39         | MS              | 195        | -1821 | 73         | C47      | 1697       | 1284 |
| 6          | C14             | -1697      | 909   | 40         | CLK2            | 345        | -1821 | 74         | C46      | 1697       | 1409 |
| 7          | C13             | -1697      | 784   | 41         | CLK1            | 495        | -1821 | 75         | C45      | 1697       | 1534 |
| 8          | C12             | -1697      | 659   | 42         | NC              |            |       | 76         | C44      | 1500       | 1822 |
| 9          | C11             | -1697      | 534   | 43         | FRM             | 645        | -1821 | 77         | C43      | 1375       | 1822 |
| 10         | C10             | -1697      | 409   | 44         | M               | 795        | -1821 | 78         | C42      | 1250       | 1822 |
| 11         | C9              | -1697      | 284   | 45         | NC              |            |       | 79         | C41      | 1125       | 1822 |
| 12         | C8              | -1697      | 159   | 46         | PCLK2           | 945        | -1821 | 80         | C40      | 1000       | 1822 |
| 13         | C7              | -1697      | 34    | 47         | DIO2            | 1095       | -1821 | 81         | C39      | 875        | 1822 |
| 14         | C6              | -1697      | -91   | 48         | NC              |            |       | 82         | C38      | 750        | 1822 |
| 15         | C5              | -1697      | -216  | 49         | CL2             | 1245       | -1821 | 83         | C37      | 625        | 1822 |
| 16         | C4              | -1697      | -341  | 50         | NC              |            |       | 84         | C36      | 500        | 1822 |
| 17         | C3              | -1697      | -466  | 51         | V0R             | 1697       | -1466 | 85         | C35      | 375        | 1822 |
| 18         | C2              | -1697      | -591  | 52         | V5R             | 1697       | -1341 | 86         | C34      | 250        | 1822 |
| 19         | C1              | -1697      | -716  | 53         | V4R             | 1697       | -1216 | 87         | C33      | 125        | 1822 |
| 20         | V <sub>EE</sub> | -1697      | -841  | 54         | V1R             | 1697       | -1091 | 88         | C32      | 0          | 1822 |
| 21         | V1L             | -1697      | -966  | 55         | V <sub>EE</sub> | 1697       | -966  | 89         | C31      | -125       | 1822 |
| 22         | V4L             | -1697      | -1091 | 56         | C64             | 1697       | -841  | 90         | C30      | -250       | 1822 |
| 23         | V5L             | -1697      | -1216 | 57         | C63             | 1697       | -716  | 91         | C29      | -375       | 1822 |
| 24         | V0L             | -1697      | -1341 | 58         | C62             | 1697       | -591  | 92         | C28      | -500       | 1822 |
| 25         | V <sub>DD</sub> | -1697      | -1466 | 59         | C61             | 1697       | 466   | 93         | C27      | -625       | 1822 |
| 26         | DIO1            | -1245      | -1821 | 60         | C60             | 1697       | -341  | 94         | C26      | -750       | 1822 |
| 27         | FS              | -1095      | -1821 | 61         | C59             | 1697       | -216  | 95         | C25      | -875       | 1822 |
| 28         | DS1             | -945       | -1821 | 62         | C58             | 1697       | -91   | 96         | C24      | -1000      | 1822 |
| 29         | DS2             | -795       | -1821 | 63         | C57             | 1697       | 34    | 97         | C23      | -1125      | 1822 |



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|    |    |      |       |    |     |      |     |     |     |       |      |
|----|----|------|-------|----|-----|------|-----|-----|-----|-------|------|
| 30 | C  | -645 | -1821 | 64 | C56 | 1697 | 159 | 98  | C22 | -1250 | 1822 |
| 31 | NC |      |       | 65 | C55 | 1697 | 284 | 99  | C21 | -1375 | 1822 |
| 32 | R  | -495 | -1821 | 66 | C54 | 1697 | 409 | 100 | C20 | -1500 | 1822 |
| 33 | NC |      |       | 67 | C53 | 1697 | 534 |     |     |       |      |
| 34 | CR | -345 | -1821 | 68 | C52 | 1697 | 659 |     |     |       |      |

## PIN DESCRIPTION

Table 1. Pin Description

| Pin Number<br>QFP (TQFP)   | Symbol   | I/O   | Description   |              |                         |                            |                                      |   |                                       |
|--|--|-------|---|--------------|-------------------------|----------------------------|--------------------------------------|---|---------------------------------------|
| 28(25)<br>40(37)<br>23(20), 58(55)                                   | $V_{DD}$<br>$V_{SS}$<br>$V_{EE}$   | Power | For internal logic circuit (+5V ± 10%)<br>GND (= 0 V)<br>For LCD driver circuit   |              |                         |                            |                                      |   |                                       |
| 27(24), 54(51)<br>24(21), 57(54)<br>25(22), 56(53)<br>26(23), 55(52) | $V_{0L}$ , $V_{0R}$<br>$V_{1L}$ , $V_{1R}$<br>$V_{4L}$ , $V_{4R}$<br>$V_{5L}$ , $V_{5R}$ | Power | Bias supply voltage terminals to drive LCD.<br><table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Select Level</th> <th>Non-Select Level</th> </tr> </thead> <tbody> <tr> <td><math>V_{0L}</math> (R), <math>V_{5L}</math> (R)</td> <td><math>V_{1L}</math> (R), <math>V_{4L}</math> (R)</td> </tr> </tbody> </table> <p><math>V_{0L}</math> and <math>V_{0R}</math> (<math>V_{1L}</math> &amp; <math>V_{1R}</math>, <math>V_{4L}</math> &amp; <math>V_{4R}</math>, <math>V_{5L}</math> &amp; <math>V_{5R}</math>) should be connected by the same voltage.</p> | Select Level | Non-Select Level        | $V_{0L}$ (R), $V_{5L}$ (R) | $V_{1L}$ (R), $V_{4L}$ (R)           |   |                                       |
| Select Level   | Non-Select Level   |       |   |              |                         |                            |                                      |   |                                       |
| $V_{0L}$ (R), $V_{5L}$ (R)   | $V_{1L}$ (R), $V_{4L}$ (R)   |       |   |              |                         |                            |                                      |   |                                       |
| 42(39)   | MS   | Input | Selection of master/slave mode<br>- Master mode (MS = 1)<br>DIO1, DIO2, CL2 and M is output state.<br>- Slave mode (MS = 0)<br>SHL = 1 → DIO1 is input state (DIO2 is output state)<br>SHL = 0 → DIO2 is input state (DIO1 is output state)<br>CL2 and M are input state.   |              |                         |                            |                                      |   |                                       |
| 39(36)   | SHL  | Input | Selection of data shift direction.<br><table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SHL</th> <th>Data Shift Direction</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>DIO1 → C1 ..... C64 → DIO0</td> </tr> <tr> <td>L</td> <td>DIO2 → C64 ..... C1 → DIO0</td> </tr> </tbody> </table>  | SHL          | Data Shift Direction    | H                          | DIO1 → C1 ..... C64 → DIO0           | L | DIO2 → C64 ..... C1 → DIO0            |
| SHL  | Data Shift Direction   |       |   |              |                         |                            |                                      |   |                                       |
| H  | DIO1 → C1 ..... C64 → DIO0   |       |   |              |                         |                            |                                      |   |                                       |
| L  | DIO2 → C64 ..... C1 → DIO0   |       |   |              |                         |                            |                                      |   |                                       |
| 49(46)   | PCLK2  | Input | Selection of shift clock (CL2) phase.<br><table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PCLK2</th> <th>Shift Clock (CL2) Phase</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Data shift at the rising edge of CL2</td> </tr> <tr> <td>L</td> <td>Data shift at the falling edge of CL2</td> </tr> </tbody> </table>   | PCLK2        | Shift Clock (CL2) Phase | H                          | Data shift at the rising edge of CL2 | L | Data shift at the falling edge of CL2 |
| PCLK2  | Shift Clock (CL2) Phase  |       |   |              |                         |                            |                                      |   |                                       |
| H  | Data shift at the rising edge of CL2   |       |   |              |                         |                            |                                      |   |                                       |
| L  | Data shift at the falling edge of CL2  |       |   |              |                         |                            |                                      |   |                                       |
| 30(27)   | FS   | Input | Selection of oscillation frequency.<br>- Master mode<br>When the frame frequency is 70 Hz, the oscillation frequency should be<br>$f_{osc} = 430\text{kHz}$ at FS = 1( $V_{DD}$ )<br>$f_{osc} = 215\text{kHz}$ at FS = 0( $V_{SS}$ )<br>- Slave mode<br>Connect to $V_{DD}$ .   |              |                         |                            |                                      |   |                                       |

Table 1. Pin Description (Continued)

| Pin Number<br>QFP (TQFP)   | Symbol       | I/O               | Description   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
|----------------------------|--------------|-------------------|---|-----|-----|------|------|---|------|--------|--------|------|--------|--------|------|---|-------|--------|---|--------|-------|
| 31(28)<br>32(29)           | DS1<br>DS2   | Input             | <p>Selection of display duty.</p> <ul style="list-style-type: none"> <li>- Master mode</li> </ul> <table border="1"> <thead> <tr> <th>DS1</th> <th>DS2</th> <th>Duty</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>1/48</td> </tr> <tr> <td>L</td> <td>H</td> <td>1/64</td> </tr> <tr> <td>H</td> <td>L</td> <td>1/96</td> </tr> <tr> <td>H</td> <td>H</td> <td>1/128</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>- Slave mode<br/>Connect to <math>V_{DD}</math></li> </ul> | DS1 | DS2 | Duty | L    | L | 1/48 | L      | H      | 1/64 | H      | L      | 1/96 | H | H     | 1/128  |   |        |       |
| DS1                        | DS2          | Duty              |   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| L                          | L            | 1/48              |   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| L                          | H            | 1/64              |   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| H                          | L            | 1/96              |   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| H                          | H            | 1/128             |   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| 33(30)<br>35(32)<br>37(34) | C<br>R<br>CR |                   | <p>RC Oscillator</p> <ul style="list-style-type: none"> <li>- Master mode: Use these terminals as shown below.</li> </ul> <ul style="list-style-type: none"> <li>- Slave mode: Stop the oscillator as shown below.</li> </ul>   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| 44(41)<br>43(40)           | CLK1<br>CLK2 | Output            | <p>Operating clock output for the S6B0108</p> <ul style="list-style-type: none"> <li>- Master mode: connection to CLK1 and CLK2 of the S6B0108</li> <li>- Slave mode: open</li> </ul>   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| 46(43)                     | FRM          | Output            | <p>Synchronous frame signal.</p> <ul style="list-style-type: none"> <li>- Master mode: connection to FRM of the S6B0108</li> <li>- Slave mode: open</li> </ul>  |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| 47(44)                     | M            | Input/<br>Output  | <p>Alternating signal input for LCD driving.</p> <ul style="list-style-type: none"> <li>- Master mode: output state Connection to M of the S6B0108</li> <li>- Slave mode: input state Connection to the controller</li> </ul>   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| 52(49)                     | CL2          | Input /<br>Output | <p>Data shift clock</p> <ul style="list-style-type: none"> <li>- Master mode: output state Connection to CL of the S6B0108</li> <li>- Slave mode: input state Connection to shift clock terminal of the controller.</li> </ul>  |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| 29(26)<br>50(47)           | DIO1<br>DIO2 | Input/<br>Output  | <p>Data input/output pin of internal shift register.</p> <table border="1"> <thead> <tr> <th>MS</th> <th>DS2</th> <th>DIO1</th> <th>DIO2</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Output</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table>  | MS  | DS2 | DIO1 | DIO2 | H | H    | Output | Output | L    | Output | Output | L    | H | Input | Output | L | Output | Input |
| MS                         | DS2          | DIO1              | DIO2  |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| H                          | H            | Output            | Output  |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
|                            | L            | Output            | Output  |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
| L                          | H            | Input             | Output  |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |
|                            | L            | Output            | Input   |     |     |      |      |   |      |        |        |      |        |        |      |   |       |        |   |        |       |

Table 1. Pin Description (Continued)

| Pin Number<br>QFP (TQFP)   | Symbol | I/O            | Description  |      |   |     |   |   |                |   |   |                |   |   |                |   |   |                |
|--|--------|----------------|--|------|---|-----|---|---|----------------|---|---|----------------|---|---|----------------|---|---|----------------|
| 22-1(19-1)<br>100-59(100-56)   | C1-C64 | Output         | Common signal output for LCD driving.<br><table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Data</th> <th>M</th> <th>Out</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>V<sub>1</sub></td> </tr> <tr> <td>L</td> <td>H</td> <td>V<sub>4</sub></td> </tr> <tr> <td>H</td> <td>L</td> <td>V<sub>5</sub></td> </tr> <tr> <td>H</td> <td>H</td> <td>V<sub>0</sub></td> </tr> </tbody> </table> | Data | M | Out | L | L | V <sub>1</sub> | L | H | V <sub>4</sub> | H | L | V <sub>5</sub> | H | H | V <sub>0</sub> |
| Data   | M      | Out            |  |      |   |     |   |   |                |   |   |                |   |   |                |   |   |                |
| L  | L      | V <sub>1</sub> |  |      |   |     |   |   |                |   |   |                |   |   |                |   |   |                |
| L  | H      | V <sub>4</sub> |  |      |   |     |   |   |                |   |   |                |   |   |                |   |   |                |
| H  | L      | V <sub>5</sub> |  |      |   |     |   |   |                |   |   |                |   |   |                |   |   |                |
| H  | H      | V <sub>0</sub> |  |      |   |     |   |   |                |   |   |                |   |   |                |   |   |                |
| 34(31), 36(33)<br>38(35), 41(38)<br>45(42), 48(45)<br>51(48), 53(50) | NC     |                | No connection  |      |   |     |   |   |                |   |   |                |   |   |                |   |   |                |

## MAXIMUM ABSOLUTE LIMIT

| Characteristic        | Symbol           | Value  | Unit | Note     |
|-----------------------|------------------|--|------|----------|
| Operating voltage     | V <sub>DD</sub>  | -0.3 - +7.0                                  | V    | (1)      |
| Supply voltage        | V <sub>EE</sub>  | V <sub>DD</sub> -19.0 - V <sub>DD</sub> +0.3 | V    | (4)      |
| Driver supply voltage | V <sub>B</sub>   | -0.3 - V <sub>DD</sub> +0.3                  | V    | (1), (2) |
|                       | V <sub>LCD</sub> | V <sub>EE</sub> -0.3 - V <sub>DD</sub> +0.3  | V    | (3), (4) |
| Operating temperature | T <sub>OPR</sub> | -30 - +85                                    | °C   | -        |
| Storage temperature   | T <sub>STG</sub> | -55 - +125                                   | °C   | -        |

## NOTES:

- Based on V<sub>SS</sub> = 0V
- Applies to input terminals and I/O terminals at high impedance. (Except V0L(R), V1L(R), V4L(R) and V5L(R)).
- Applies to V0L(R), V1L(R), V4L(R) and V5L(R).
- Voltage level: V<sub>DD</sub> ≥ V0L = V0R ≥ V1L = V1R ≥ V4L = V4R ≥ V5L = V5R ≥ V<sub>EE</sub>.

## ELECTRICAL CHARACTERISTICS

### DC CHARACTERISTICS

( $V_{DD} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $|V_{DD}-V_{EE}|=8 - 17V$ ,  $T_a = -30$  to  $+85^\circ C$ )

| Characteristic          |      | Symbol    | Condition  | Min          | Typ | Max         | Unit       | Note |
|-------------------------|------|-----------|--|--------------|-----|-------------|------------|------|
| Input Voltage           | High | $V_{IH}$  | -  | $0.7V_{DD}$  | -   | $V_{DD}$    | V          | (1)  |
|                         | Low  | $V_{IL}$  |  | $V_{SS}$     | -   | $0.3V_{DD}$ |            |      |
| Output Voltage          | High | $V_{OH}$  | $I_{OH} = -0.4mA$                                      | $V_{DD}-0.4$ | -   | -           | V          | (2)  |
|                         | Low  | $V_{OL}$  | $I_{OL} = 0.4mA$                                       | -            | -   | 0.4         |            |      |
| Input leakage current   |      | $I_{LKG}$ | $V_{IN} = V_{DD}-V_{SS}$                               | -1.0         | -   | 1.0         | $\mu A$    | (1)  |
| OSC frequency           |      | $f_{OSC}$ | $R_f = 47k\Omega \pm 2\%$<br>$C_f = 20pf \pm 5\%$      | 315          | 450 | 585         | kHz        |      |
| On resistance (VDIV-Cl) |      | $R_{ON}$  | $V_{DD}-V_{EE} = 17V$<br>Load current = $\pm 150\mu A$ | -            | -   | 1.5         | K $\Omega$ |      |
| Operating current       |      | $I_{DD1}$ | Master mode<br>1/128 Duty                              | -            | -   | 1.0         | mA         | (3)  |
|                         |      | $I_{DD2}$ | Slave mode<br>1/128 Duty                               | -            | -   | 200         | $\mu A$    | (4)  |
| Supply current          |      | $I_{EE}$  | Master mode<br>1/128 Duty                              | -            | -   | 100         |            | (5)  |
| Operating Frequency     |      | $f_{op1}$ | Master mode<br>External clock                          | 50           | -   | 600         | kHz        |      |
|                         |      | $f_{op2}$ | Slave mode   | 0.5          | -   | 1500        |            |      |

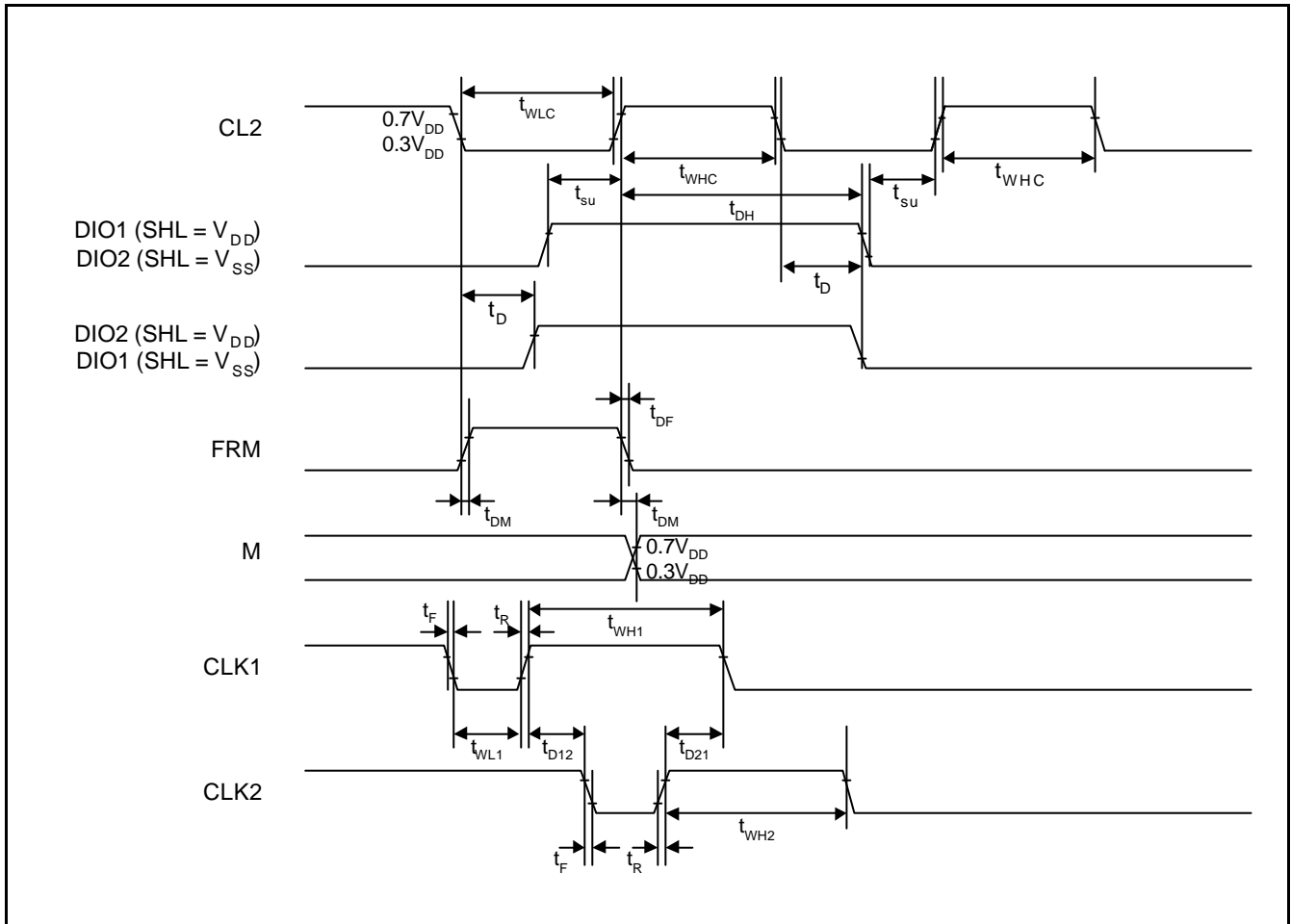
#### NOTES:

1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the output state.
3. This value is specified at about the current flowing through  $V_{SS}$ . Internal oscillation circuit:  $R_f = 47k\Omega$ ,  $C_f = 20pF$  Each terminal of DS1, DS2, FS, SHL and MS is connected to  $V_{DD}$  and out is no load.
4. This value is specified at about the current flowing through  $V_{SS}$ . Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to  $V_{DD}$ , and MS is connected to  $V_{SS}$ . CL2, M, DIO1 is external clock.
5. This value is specified at about the current flowing through  $V_{EE}$ . Don't connect to  $V_{LCD}$  (V1-V5).

**AC CHARACTERISTICS ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = -30^\circ C$  to  $+85^\circ C$ )**

**Master Mode**

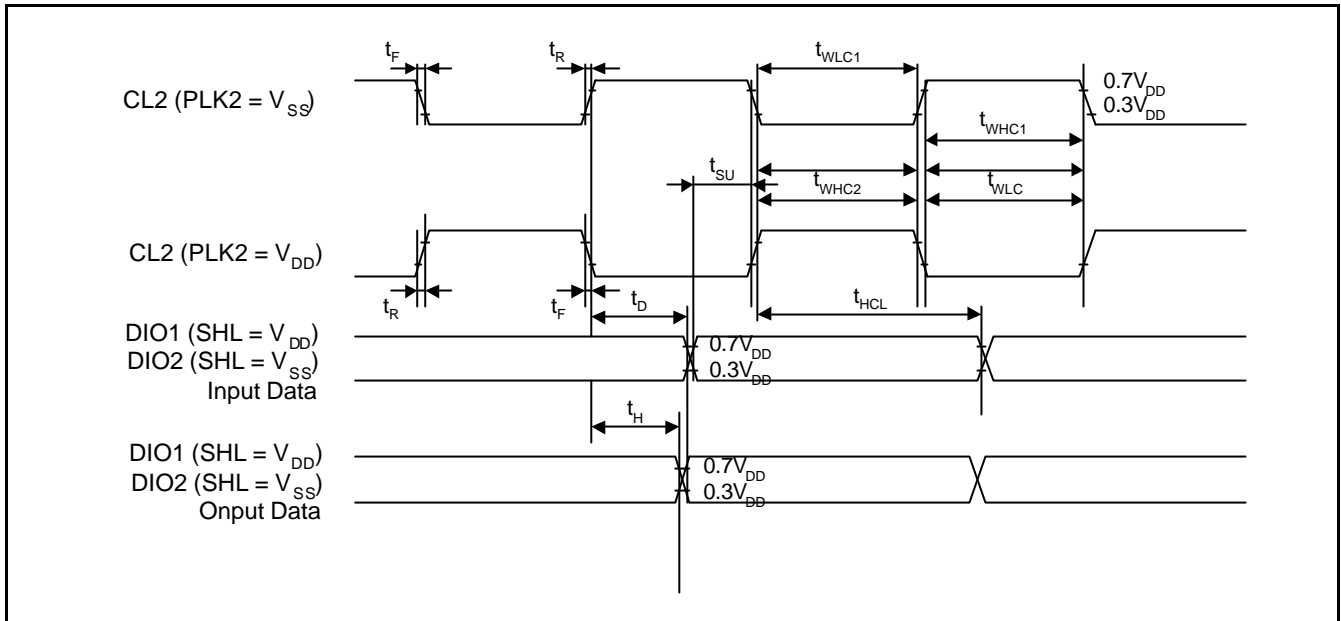
( $MS = V_{DD}$ ,  $PCLK2 = V_{DD}$ ,  $C_f = 20pF$ ,  $R_f = 47k\Omega$ )



**Master Mode**

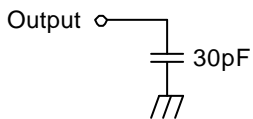
| Characteristic             | Symbol    | Min  | Typ | Max | Unit    |
|----------------------------|-----------|------|-----|-----|---------|
| Data setup time            | $t_{SU}$  | 20   | –   | –   | $\mu s$ |
| Data hold time             | $t_{DH}$  | 40   | –   | –   |         |
| Data delay time            | $t_D$     | 5    | –   | –   |         |
| FRM delay time             | $t_{DF}$  | -2   | –   | 2   |         |
| M delay time               | $t_{DM}$  | -2   | –   | 2   |         |
| CL2 low level width        | $t_{WLC}$ | 35   | –   | –   |         |
| CL2 high level width       | $t_{WHC}$ | 35   | –   | –   | ns      |
| CLK1 low level width       | $t_{WL1}$ | 700  | –   | –   |         |
| CLK2 low level width       | $t_{WL2}$ | 700  | –   | –   |         |
| CLK1 high level width      | $t_{WH1}$ | 2100 | –   | –   |         |
| CLK2 high level width      | $t_{WH2}$ | 2100 | –   | –   |         |
| CLK1-CLK2 phase difference | $t_{D12}$ | 700  | –   | –   |         |
| CLK2-CLK1 phase difference | $t_{D21}$ | 700  | –   | –   |         |
| CLK1, CLK2 rise/fall time  | $t_R/t_F$ | –    | –   | 150 |         |

Slave Mode (MS = V<sub>SS</sub>)



| Characteristics       | Symbol                         | Min | Typ | Max | Unit | Note                    |
|-----------------------|--------------------------------|-----|-----|-----|------|-------------------------|
| CL2 low level width   | t <sub>WLC1</sub>              | 450 | –   | –   | ns   | PCLK2 = V <sub>SS</sub> |
| CL2 high level width  | t <sub>WHC1</sub>              | 150 | –   | –   | ns   | PCLK2 = V <sub>SS</sub> |
| CL2 low level width   | t <sub>WLC2</sub>              | 150 | –   | –   | ns   | PCLK2 = V <sub>DD</sub> |
| CL2 high level width  | t <sub>WHL</sub>               | 450 | –   | –   | ns   | PCLK2 = V <sub>DD</sub> |
| Data setup time       | t <sub>SU</sub>                | 100 | –   | –   | ns   |                         |
| Data hold time        | t <sub>DH</sub>                | 100 | –   | –   | ns   |                         |
| Data delay time       | t <sub>D</sub>                 | –   | –   | 200 | ns   | (NOTE)                  |
| Output data hold time | t <sub>H</sub>                 | 10  | –   | –   | ns   |                         |
| CL2 rise/fall time    | t <sub>R</sub> /t <sub>F</sub> | –   | –   | 30  | ns   |                         |

**NOTE:** Connect load CL = 30pF





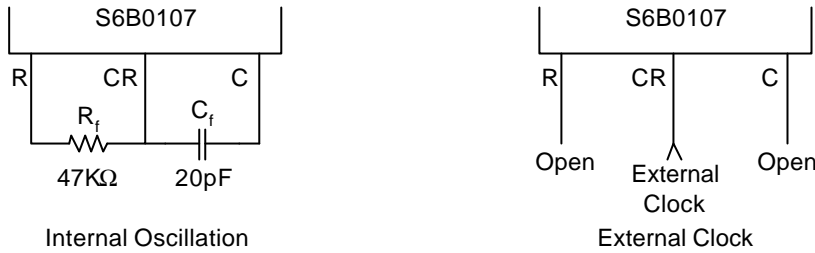
**FUNCTIONAL DESCRIPTION**

**RC Oscillator**

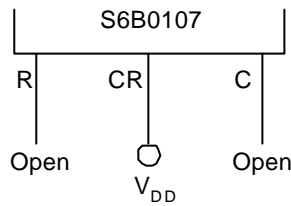
The RC Oscillator generates CL2, M, FRM of the S6B0107, and CLK1 and CLK2 of the S6B0108 by the oscillation resistor R and capacitor C.

When selecting the master/slave mode, the oscillation circuit is as following:

Master Mode: In the master mode, use these terminals as shown below.



Slave Mode: In the slave mode, stop the oscillator as shown below.



**Timing Generation Circuit**

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

Selection of Master/Slave (M/S) Mode

- When M/S is "H", it generates CL2, M, FRM, CLK1 and CLK2 internally.
- When M/S is "L", it operates by receiving M and CL2 from the mater device

Frequency Selection (FS)

To adjust FRM frequency by 70Hz, the oscillation frequency should be as follows:

| FS | Oscillation Frequency |
|----|-----------------------|
| H  | $f_{OSC} = 430kHz$    |
| L  | $f_{OSC} = 215kHz$    |

In the slave mode, it is connected to  $V_{DD}$ .

## Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

| DS1 | DS2 | DUTY  |
|-----|-----|-------|
| L   | L   | 1/48  |
|     | H   | 1/64  |
| H   | L   | 1/96  |
|     | H   | 1/128 |

## Data Shift &amp; Phase Select Control

## Phase Selection

It is a circuit to shift data on synchronization or rising edge, or falling edge of the CL2 according to PCLK2.

| PCLK2 | Phase Selection                   |
|-------|-----------------------------------|
| H     | Data shift on rising edge of CL2  |
| L     | Data shift on falling edge of CL2 |

## Data Shift Direction Selection

When M/S is connected to  $V_{DD}$ , DIO1 and DIO2 terminal is only output.

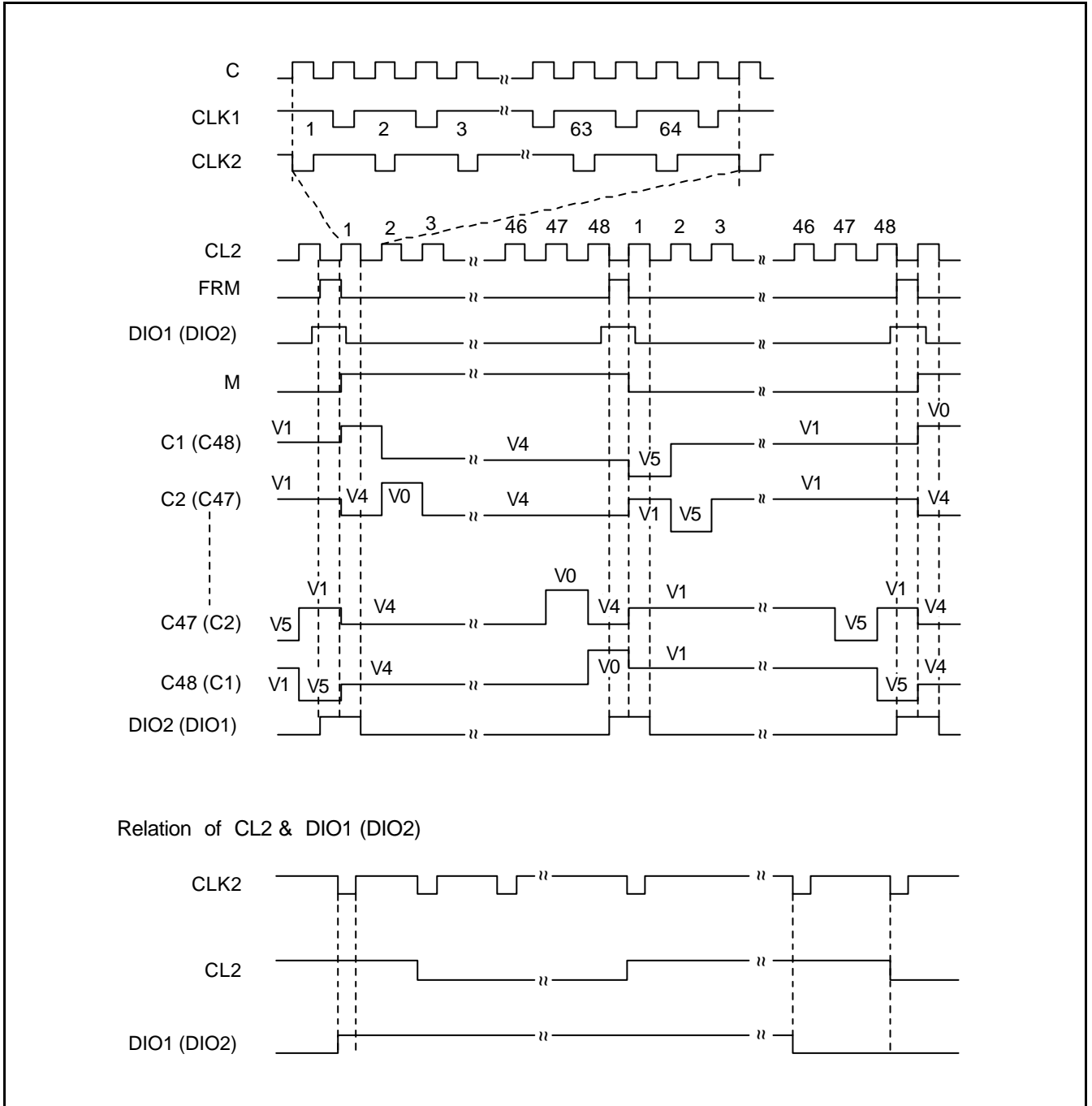
When M/S is connected to  $V_{SS}$ , it depends on the SHL.

| MS | SHL | DIO1   | DIO2   | Direction of Data      |
|----|-----|--------|--------|------------------------|
| H  | H   | Output | Output | C1 → C64               |
|    | L   | Output | Output | C64 → C1               |
| L  | H   | Input  | Output | DIO1 → C1 → C64 → DIO2 |
|    | L   | Output | Input  | DIO2 → C64 → C1 → DIO1 |

**TIMING DIAGRAM**

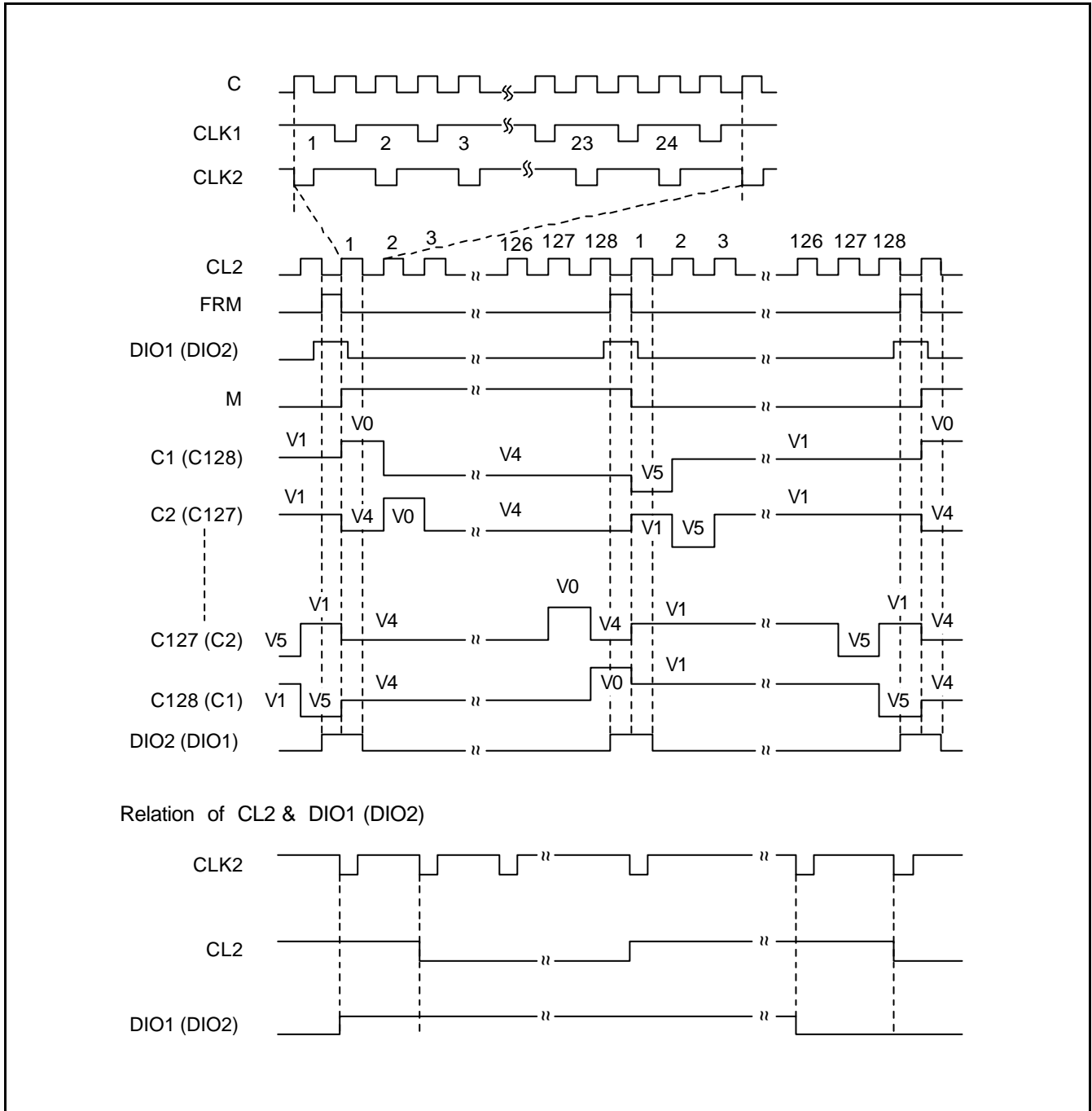
**1/48 DUTY TIMING (MASTER MODE)**

Condition: DS1 = L, DS2 = L, SHL = H(L), PCLK2 = H



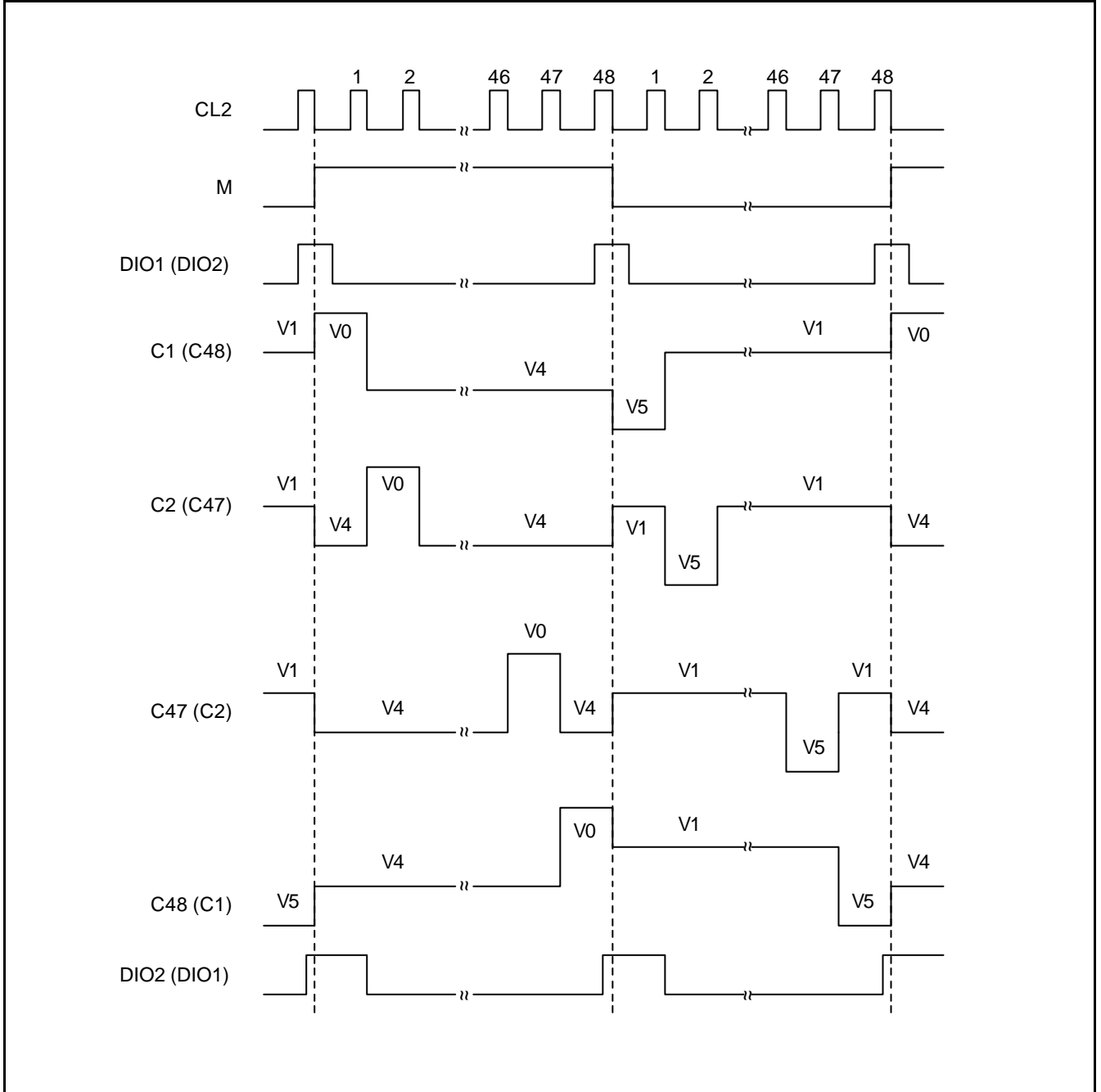
1/128 DUTY TIMING (MASTER MODE)

Condition: DS1 = H, DS2 = H, SHL = H(L), PCLK2 = H

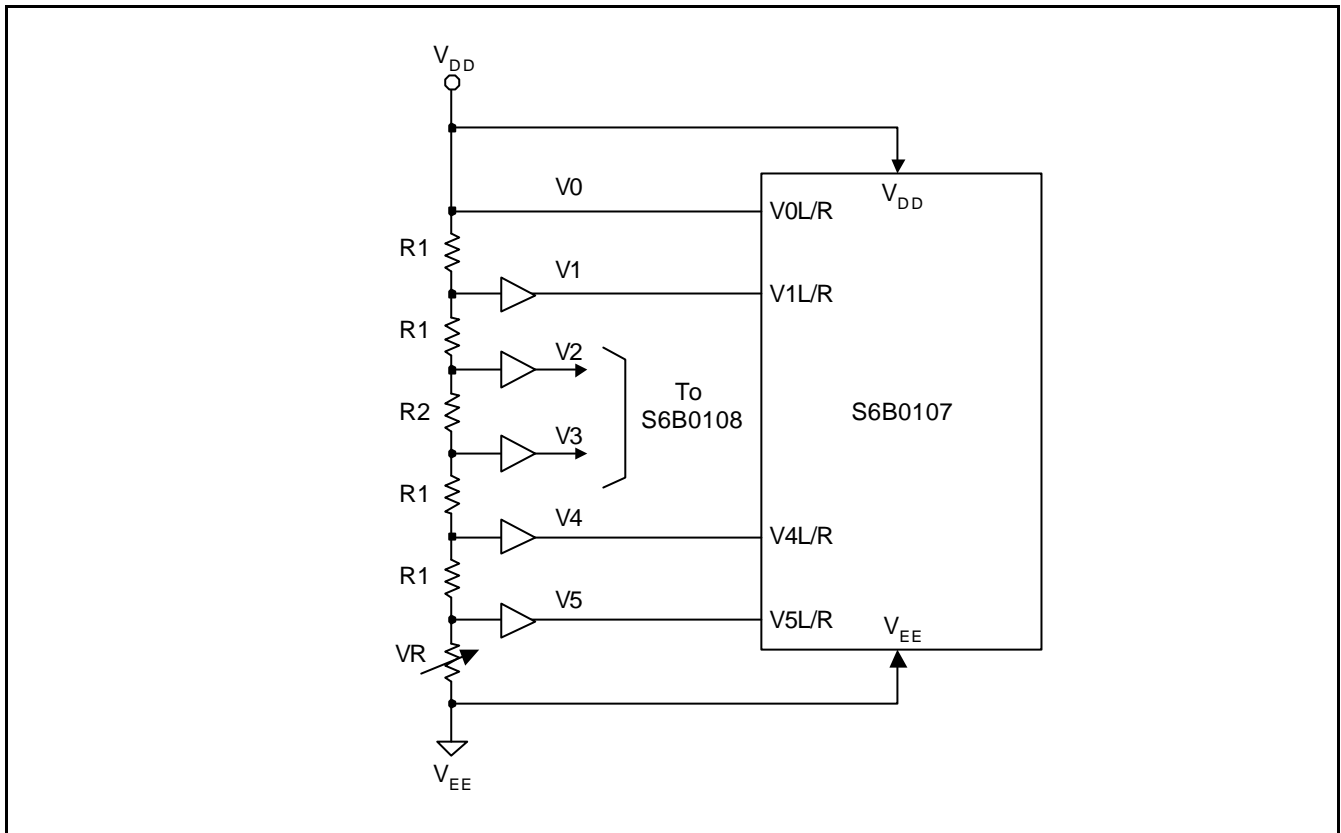


1/48 DUTY TIMING (SLAVE MODE)

Condition: PCLK2 = L, SHL = H(L)



POWER DRIVER CIRCUIT



Relation of Duty & Bias

| Duty  | Bias | RDIV     |
|-------|------|----------|
| 1/48  | 1/8  | R2 = 4R1 |
| 1/64  | 1/9  | R2 = 5R1 |
| 1/96  | 1/11 | R2 = 7R1 |
| 1/128 | 1/12 | R2 = 8R1 |

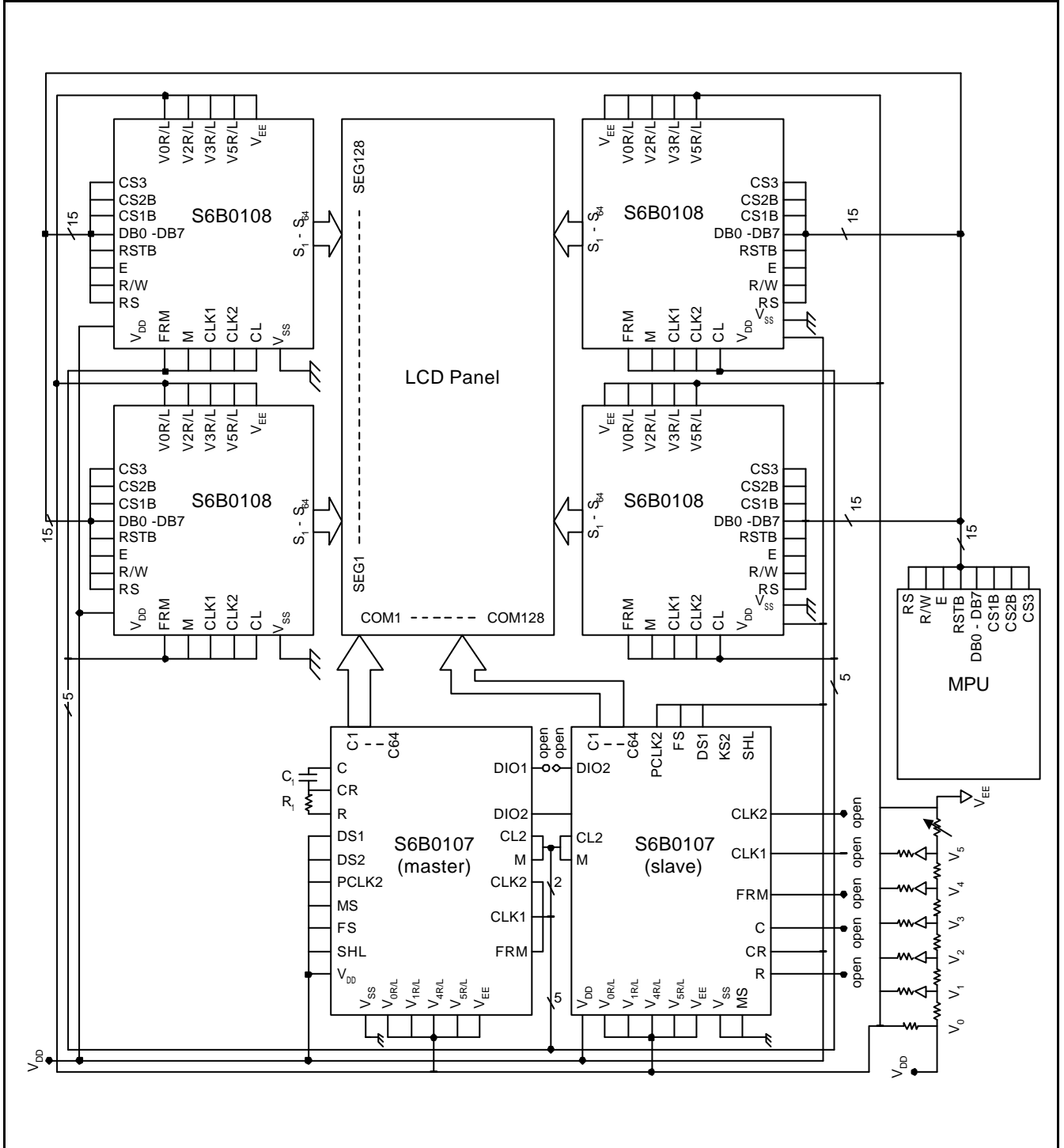
When duty factor is 1/48, the value of R1 & R2 should satisfy.

$$R1 / (4R1 + R2) = 1/8$$

$$R1 = 3k\Omega, R2 = 12k\Omega$$

APPLICATION CIRCUIT

1/128 duty segment drive (S6B0108) interface circuit





## APPENDIX D: SAMSUNG S6B0108 64 CH SEGMENT DRIVER

---

The complete Samsung's *S6B0108 64 CH Segment Driver for Dot Matrix LCD* specifications follows.



# S6B0108

## 64CH SEGMENT DRIVER FOR DOT MATRIX LCD

July. 2001

Ver. 0.0

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### **Precautions for Light**

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

| S6B0755 Specification Revision History |          |           |
|--|----------|-----------|
| Version                                | Content  | Date      |
| 0.0                                    | Original | July.2001 |

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## INTRODUCTION

The S6B0108 (TQFP type: S6B2108) is a LCD driver LSI with 64 channel output for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64 bit data latch, 64 bit drivers and decoder logic. It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The S6B0108 composed of the liquid crystal display system in combination with the S6B0107 (64 channel common driver -TQFP type: S6B2107).

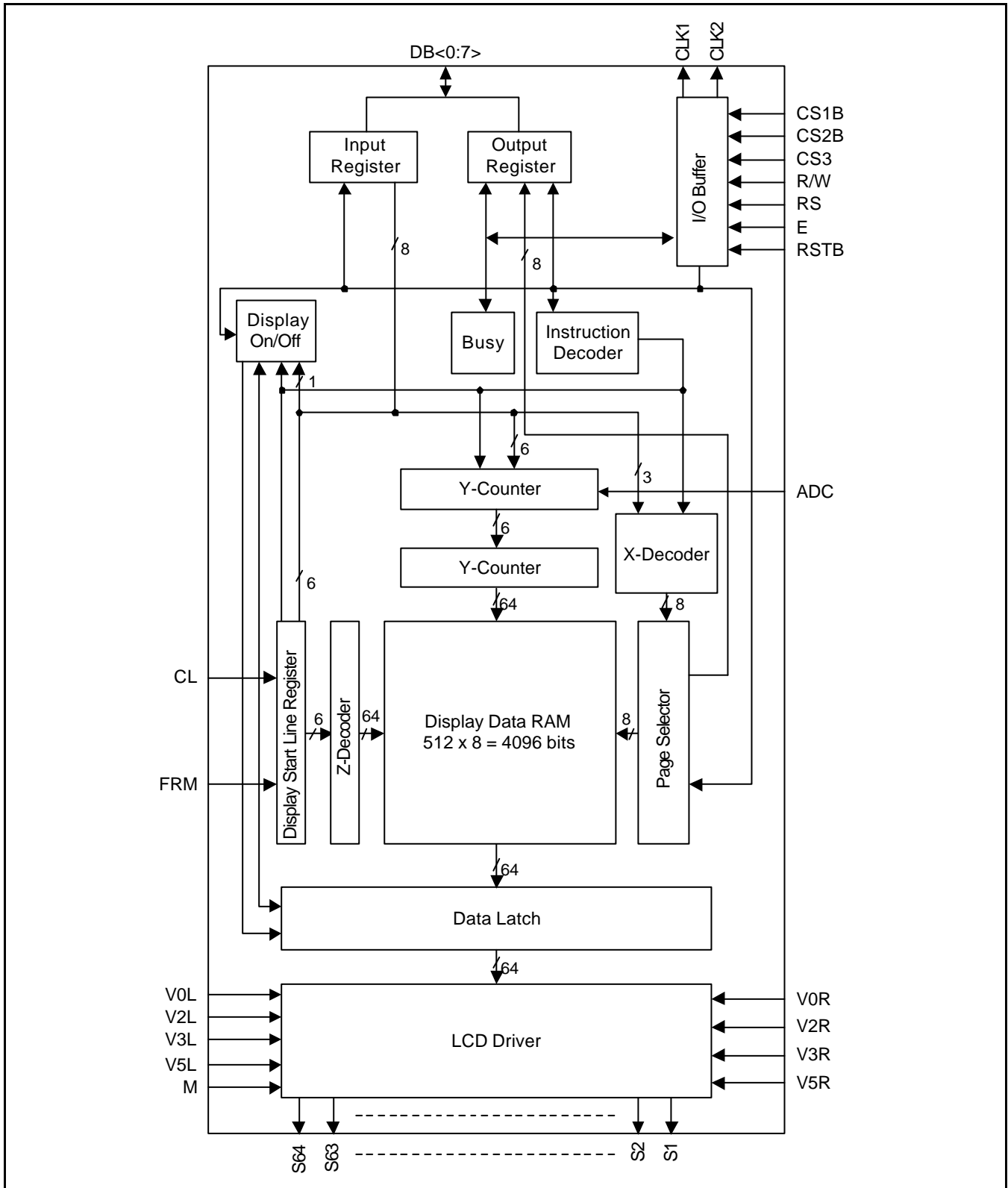
## FEATURES

- Dot matrix LCD segment driver with 64 channel output
- Input and output signal
  - Input: 8 bit parallel display data control signal from MPU divided bias voltage (V0R, V0L, V2R, V2L, V3R, V3L, V5R, V5L)
  - Output: 64 channel for LCD driving.
- Display data is stored in display data RAM from MPU.
- Interface RAM
  - Capacity: 512 bytes (4096 bits)
  - RAM bit data: RAM bit data = 1: On  
RAM bit data = 0: Off
- Applicable LCD duty: 1/32-1/64
- LCD driving voltage: 8V-17V ( $V_{DD}-V_{EE}$ )
- Power supply voltage: + 5V  $\pm$  10%
- Interface

| Drivers |               | Controller |
|---------|---------------|------------|
| Common  | Segment       |            |
| S6B0107 | Other S6B0108 | MPU        |

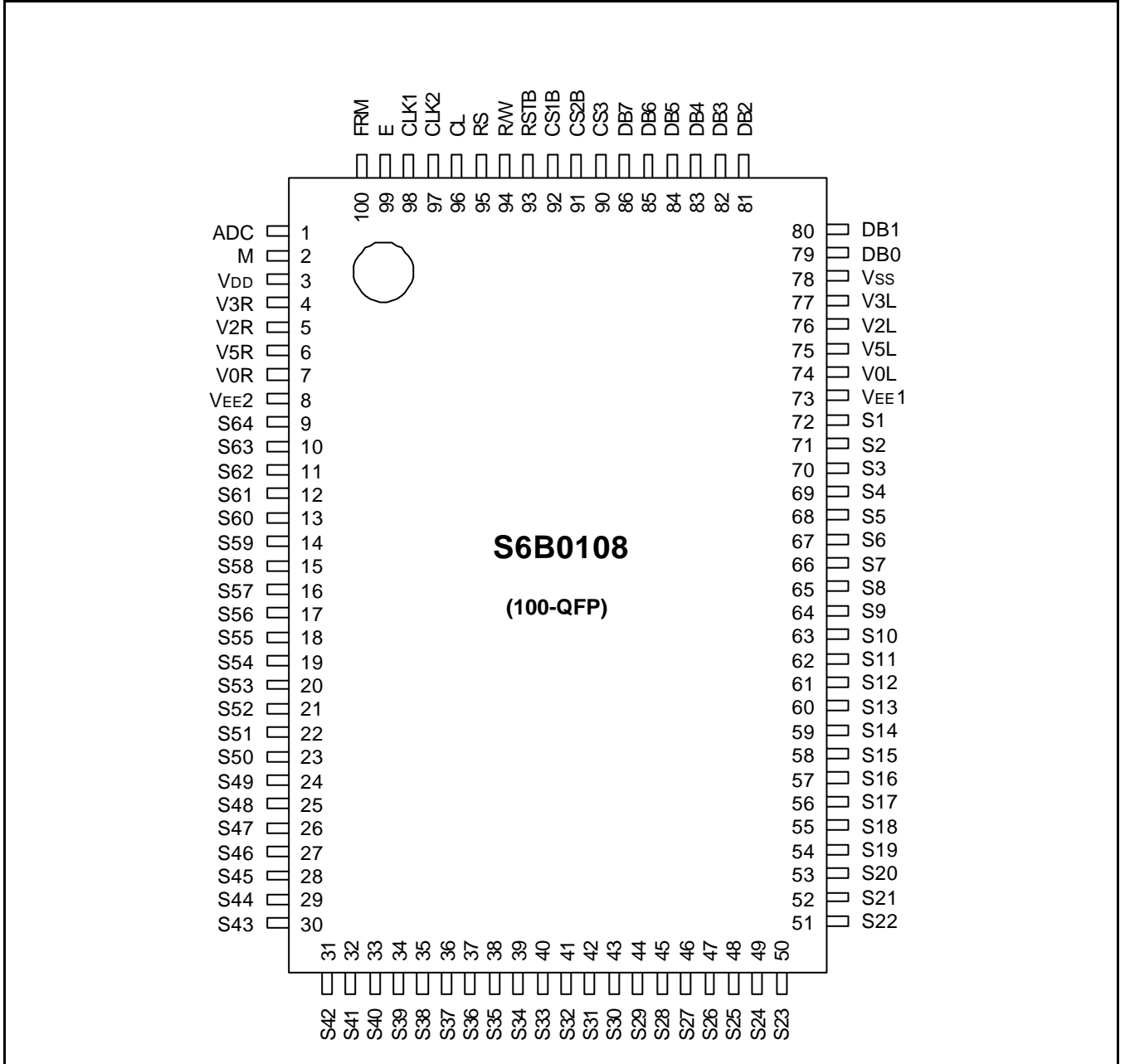
- High voltage CMOS process
- 100QFP/100TQFP or bare chip available.

BLOCK DIAGRAM

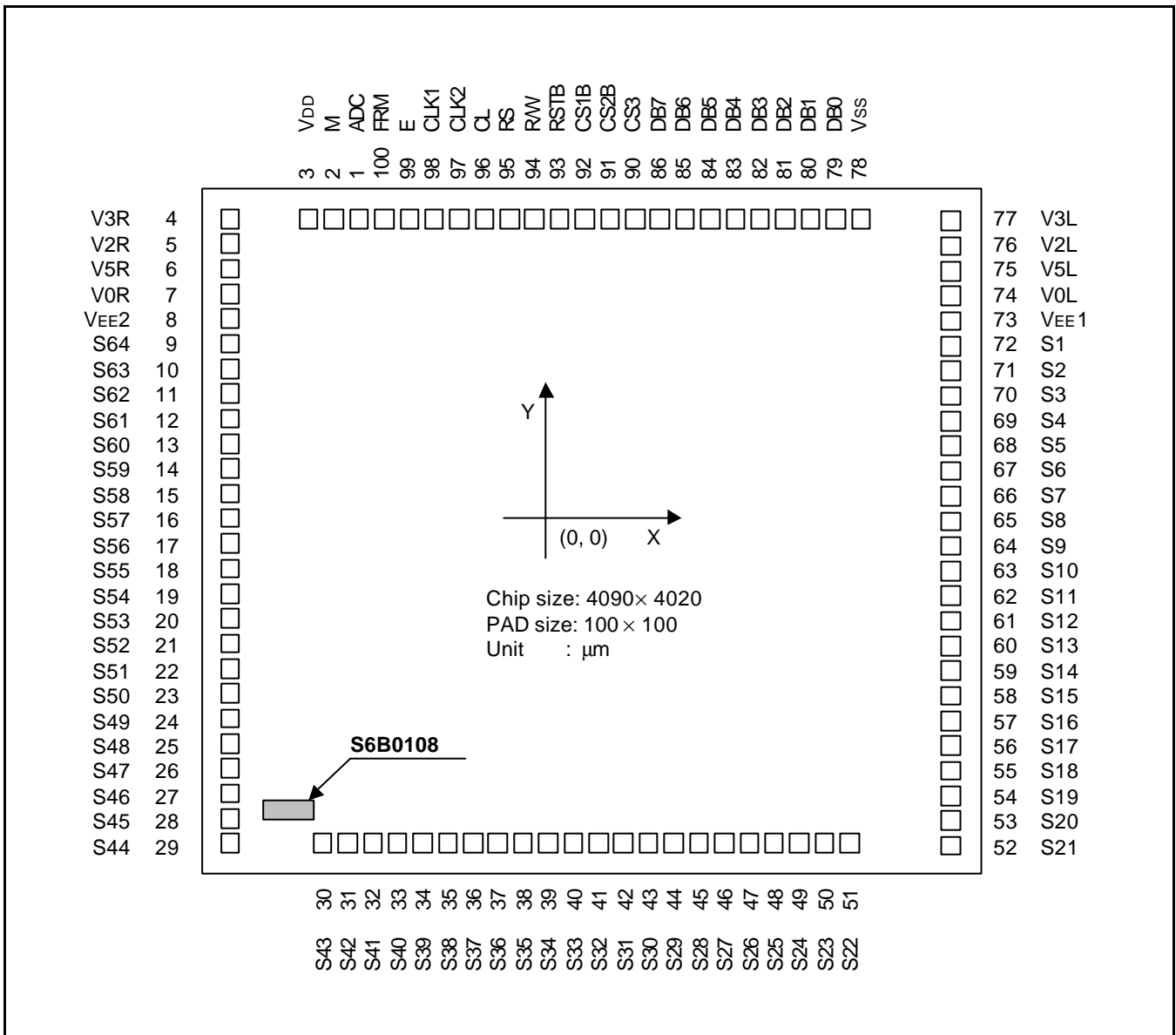


**PIN CONFIGURATION**

100 QFP



PAD DIAGRAM (CHIP LAYOUT FOR THE 100QFP)



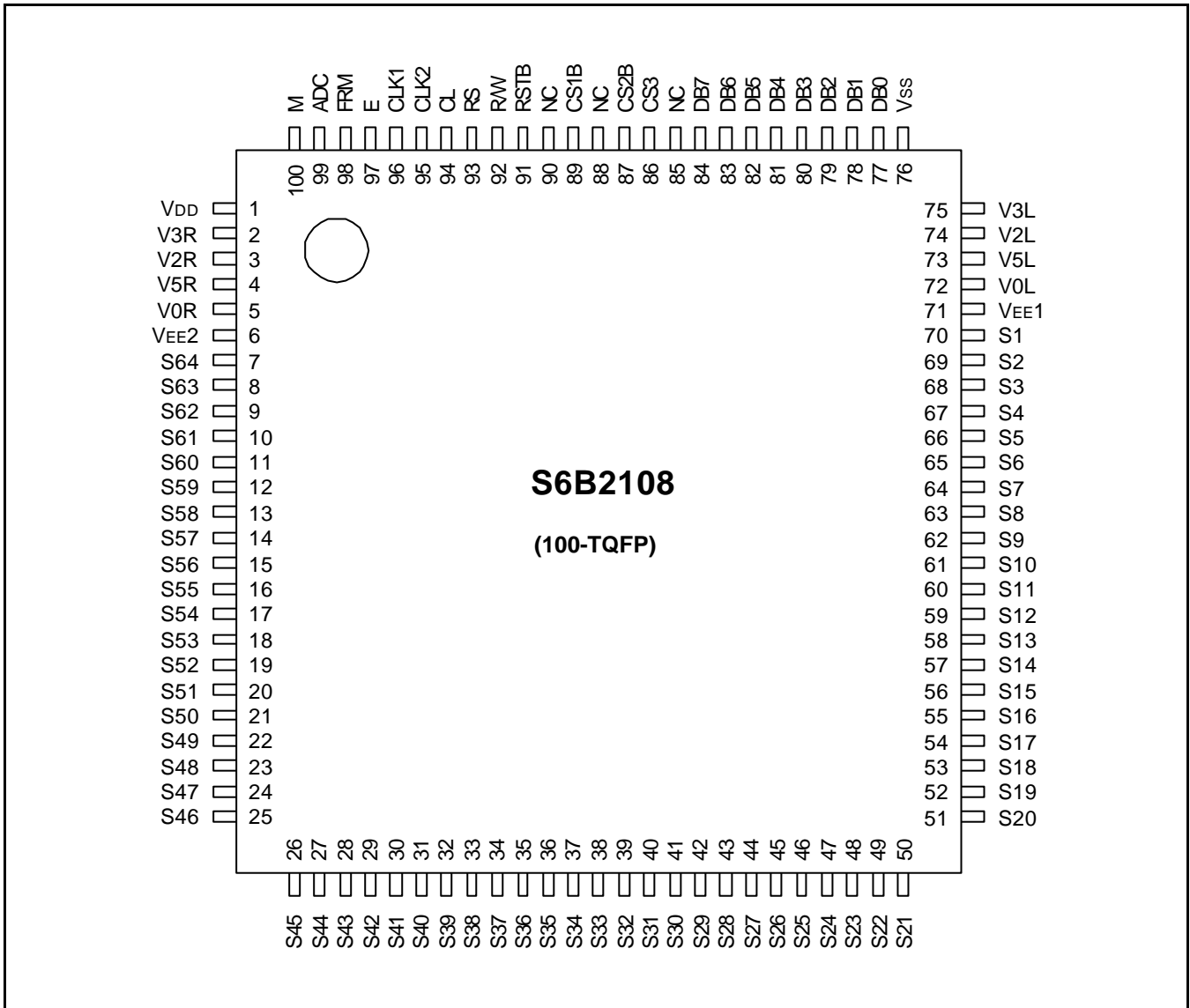
There is mark of S6B0108 on the bottom left in the chip.



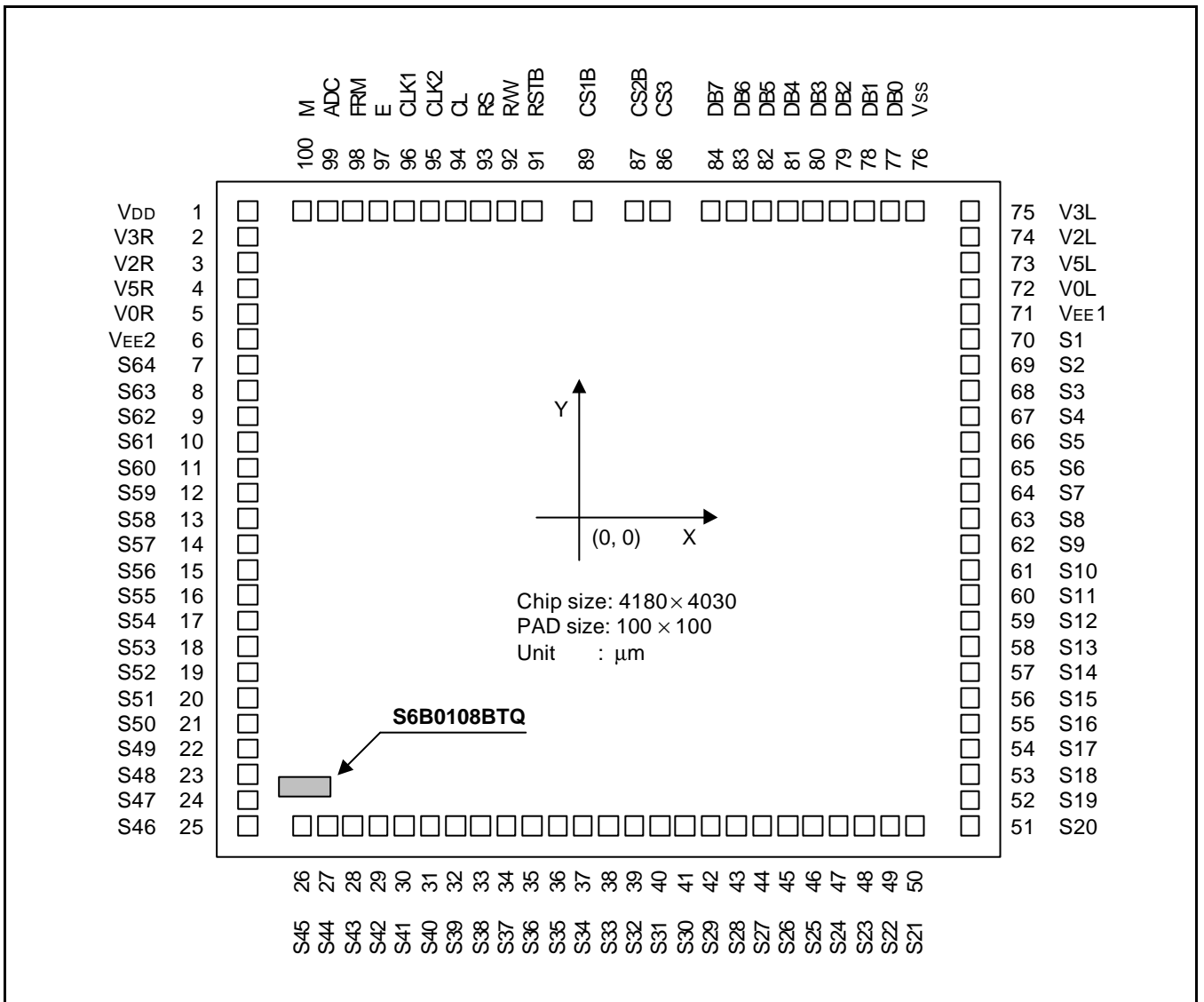
## PAD CENTER COORDINATES (100QFP)

| PAD<br>Number | PAD<br>Name      | Coordinate |       | PAD<br>Number | PAD<br>Name | Coordinate |       | PAD<br>Number | PAD<br>Name      | Coordinate |      |
|---------------|------------------|------------|-------|---------------|-------------|------------|-------|---------------|------------------|------------|------|
|               |                  | X          | Y     |               |             | X          | Y     |               |                  | X          | Y    |
| 1             | ADC              | -1140      | 1845  | 35            | S38         | -687       | -1845 | 69            | S4               | 1882       | 791  |
| 2             | M                | -1275      | 1845  | 36            | S37         | -562       | -1845 | 70            | S3               | 1882       | 916  |
| 3             | V <sub>DD</sub>  | -1410      | 1845  | 37            | S36         | -437       | -1845 | 71            | S2               | 1882       | 1041 |
| 4             | V3R              | -1882      | 1809  | 38            | S35         | -312       | -1845 | 72            | S1               | 1882       | 1166 |
| 5             | V2R              | -1882      | 1684  | 39            | S34         | -187       | -1845 | 73            | V <sub>EE1</sub> | 1882       | 1310 |
| 6             | V5R              | -1882      | 1559  | 40            | S33         | -62        | -1845 | 74            | V0L              | 1882       | 1435 |
| 7             | V0R              | -1882      | 1434  | 41            | S32         | 62         | -1845 | 75            | V5L              | 1882       | 1559 |
| 8             | V <sub>EE2</sub> | -1882      | 1309  | 42            | S31         | 187        | -1845 | 76            | V2L              | 1882       | 1684 |
| 9             | S64              | -1882      | 1165  | 43            | S30         | 312        | -1845 | 77            | V3L              | 1882       | 1809 |
| 10            | S63              | -1882      | 1040  | 44            | S29         | 437        | -1845 | 78            | V <sub>SS</sub>  | 1412       | 1845 |
| 11            | S62              | -1882      | 915   | 45            | S28         | 562        | -1845 | 79            | DB0              | 1277       | 1845 |
| 12            | S61              | -1882      | 790   | 46            | S27         | 687        | -1845 | 80            | DB1              | 1142       | 1845 |
| 13            | S60              | -1882      | 665   | 47            | S26         | 812        | -1845 | 81            | DB2              | 1007       | 1845 |
| 14            | S59              | -1882      | 540   | 48            | S25         | 937        | -1845 | 82            | DB3              | 882        | 1845 |
| 15            | S58              | -1882      | 415   | 49            | S24         | 1062       | -1845 | 83            | DB4              | 757        | 1845 |
| 16            | S57              | -1882      | 290   | 50            | S23         | 1187       | -1845 | 84            | DB5              | 632        | 1845 |
| 17            | S56              | -1882      | 165   | 51            | S22         | 1487       | -1845 | 85            | DB6              | 507        | 1845 |
| 18            | S55              | -1882      | 40    | 52            | S21         | 1882       | -1379 | 86            | DB7              | 382        | 1845 |
| 19            | S54              | -1882      | -84   | 53            | S20         | 1882       | -1239 | 90            | CS3              | 245        | 1845 |
| 20            | S53              | -1882      | -209  | 54            | S19         | 1882       | -1099 | 91            | CS2B             | 120        | 1845 |
| 21            | S52              | -1882      | -334  | 55            | S18         | 1882       | -959  | 92            | CS1B             | -5         | 1845 |
| 22            | S51              | -1882      | -459  | 56            | S17         | 1882       | -834  | 93            | RSTB             | -130       | 1845 |
| 23            | S50              | -1882      | -584  | 57            | S16         | 1882       | -709  | 94            | R/W              | -255       | 1845 |
| 24            | S49              | -1882      | -709  | 58            | S15         | 1882       | -584  | 95            | RS               | -380       | 1845 |
| 25            | S48              | -1882      | -834  | 59            | S14         | 1882       | -459  | 96            | CL               | -505       | 1845 |
| 26            | S47              | -1882      | -959  | 60            | S13         | 1882       | -334  | 97            | CLK2             | -630       | 1845 |
| 27            | S46              | -1882      | -1099 | 61            | S12         | 1882       | -209  | 98            | CLK1             | -755       | 1845 |
| 28            | S45              | -1882      | -1239 | 62            | S11         | 1882       | -84   | 99            | E                | -880       | 1845 |
| 29            | S44              | -1882      | -1379 | 63            | S10         | 1882       | 41    | 100           | FRM              | -1005      | 1845 |
| 30            | S43              | -1487      | -1845 | 64            | S9          | 1882       | 166   |               |                  |            |      |
| 31            | S42              | -1187      | -1845 | 65            | S8          | 1882       | 291   |               |                  |            |      |
| 32            | S41              | -1062      | -1845 | 66            | S7          | 1882       | 416   |               |                  |            |      |
| 33            | S40              | -937       | -1845 | 67            | S6          | 1882       | 541   |               |                  |            |      |
| 34            | S39              | -812       | -1845 | 68            | S5          | 1882       | 666   |               |                  |            |      |

100TQFP (S6B2108)



PAD DIAGRAM (CHIP LAYOUT FOR THE 100TQFP)



There is mark of S6B2108 on the bottom left in the chip.

## PAD CENTER COORDINATES (100TQFP- S6B2108)

| PAD Number | PAD Name        | Coordinate |         | PAD Number | PAD Name | Coordinate |         | PAD Number | PAD Name        | Coordinate |        |
|------------|-----------------|------------|---------|------------|----------|------------|---------|------------|-----------------|------------|--------|
|            |                 | X          | Y       |            |          | X          | Y       |            |                 | X          | Y      |
| 1          | V <sub>DD</sub> | -1924      | 1812.5  | 36         | S35      | -301.1     | -1849   | 71         | V <sub>EE</sub> | 1924       | 1312.5 |
| 2          | V3              | -1924      | 1687.5  | 37         | S34      | -173.9     | -1849   | 72         | V0              | 1924       | 1437.5 |
| 3          | V2              | -1924      | 1562.5  | 38         | S33      | -46.7      | -1849   | 73         | V5              | 1924       | 1562.5 |
| 4          | V5              | -1924      | 1437.5  | 39         | S32      | 80.5       | -1849   | 74         | V2              | 1924       | 1687.5 |
| 5          | V0              | -1924      | 1312.5  | 40         | S31      | 207.7      | -1849   | 75         | V3              | 1924       | 1812.5 |
| 6          | V <sub>EE</sub> | -1924      | 1187.5  | 41         | S30      | 334.9      | -1849   | 76         | V <sub>SS</sub> | 1450.5     | 1849   |
| 7          | S64             | -1924      | 1033.2  | 42         | S29      | 462.1      | -1849   | 77         | DB0             | 1315.5     | 1849   |
| 8          | S63             | -1924      | 906     | 43         | S28      | 589.3      | -1849   | 78         | DB1             | 1180.5     | 1849   |
| 9          | S62             | -1924      | 778.8   | 44         | S27      | 716.5      | -1849   | 79         | DB2             | 1045.5     | 1849   |
| 10         | S61             | -1924      | 651.6   | 45         | S26      | 843.7      | -1849   | 80         | DB3             | 920.5      | 1849   |
| 11         | S60             | -1924      | 524.4   | 46         | S25      | 970.9      | -1849   | 81         | DB4             | 795.5      | 1849   |
| 12         | S59             | -1924      | 397.2   | 47         | S24      | 1098.1     | -1849   | 82         | DB5             | 670.5      | 1849   |
| 13         | S58             | -1924      | 270     | 48         | S23      | 1225.3     | -1849   | 83         | DB6             | 545.5      | 1849   |
| 14         | S57             | -1924      | 142.8   | 49         | S22      | 1352.5     | -1849   | 84         | DB7             | 420.5      | 1849   |
| 15         | S56             | -1924      | 15.6    | 50         | S21      | 1479.7     | -1849   | 85         | NC              |            |        |
| 16         | S55             | -1924      | -111.6  | 51         | S20      | 1924       | -1245.3 | 86         | CS3             | 282.8      | 1849   |
| 17         | S54             | -1924      | -238.8  | 52         | S19      | 1924       | -1118.1 | 87         | CS2B            | 157.8      | 1849   |
| 18         | S53             | -1924      | -366    | 53         | S18      | 1924       | -990.9  | 88         | NC              |            |        |
| 19         | S52             | -1924      | -493.2  | 54         | S17      | 1924       | -863.7  | 89         | CS1B            | 32.8       | 1849   |
| 20         | S51             | -1924      | -620.4  | 55         | S16      | 1924       | -736.5  | 90         | NC              |            |        |
| 21         | S50             | -1924      | -747.6  | 56         | S15      | 1924       | -609.3  | 91         | RSTB            | -92.2      | 1849   |
| 22         | S49             | -1924      | -874.8  | 57         | S14      | 1924       | -482.1  | 92         | RW              | -217.2     | 1849   |
| 23         | S48             | -1924      | -1002   | 58         | S13      | 1924       | -354.9  | 93         | RS              | -342.2     | 1849   |
| 24         | S47             | -1924      | -1129.2 | 59         | S12      | 1924       | -227.7  | 94         | CL              | 467.2      | 1849   |
| 25         | S46             | -1924      | -1256.4 | 60         | S11      | 1924       | -100.5  | 95         | CLK2            | -592.2     | 1849   |
| 26         | S45             | -1573.1    | -1849   | 61         | S10      | 1924       | 26.7    | 96         | CLK1            | -717.2     | 1849   |
| 27         | S44             | -1445.9    | -1849   | 62         | S9       | 1924       | 153.9   | 97         | E               | -842.2     | 1849   |
| 28         | S43             | -1318.7    | -1849   | 63         | S8       | 1924       | 281.1   | 98         | FRW             | -967.2     | 1849   |
| 29         | S42             | -1191.5    | -1849   | 64         | S7       | 1924       | 408.3   | 99         | ADC             | -1177.8    | 1849   |
| 30         | S41             | -1064.3    | -1849   | 65         | S6       | 1924       | 535.5   | 100        | M               | -1312.8    | 1849   |
| 31         | S40             | -937.1     | -1849   | 66         | S5       | 1924       | 662.7   |            |                 |            |        |
| 32         | S39             | -809.9     | -1849   | 67         | S4       | 1924       | 789.9   |            |                 |            |        |
| 33         | S38             | -682.7     | -1849   | 68         | S3       | 1924       | 917.1   |            |                 |            |        |
| 34         | S37             | -555.5     | -1849   | 69         | S2       | 1924       | 1044.3  |            |                 |            |        |
| 35         | S36             | -428.3     | -1849   | 70         | S1       | 1924       | 1171.5  |            |                 |            |        |

## PIN DESCRIPTION

Table 1. Pin Description

| Pin Number<br>QFP(TQFP)                                      | Symbol   | Input/Output | Description   |              |                  |                           |                           |
|--|--|--------------|---|--------------|------------------|---------------------------|---------------------------|
| 3(1)<br>78(76)<br>73(71), 8(6)                               | $V_{DD}$<br>$V_{SS}$<br>$V_{EE1,2}$  | Power        | For internal logic circuit (+5V $\pm$ 10%)<br>GND (0V)<br>For LCD driver circuit<br>$V_{SS} = 0V$ , $V_{DD} = +5V \pm 10\%$ , $V_{DD} - V_{EE} = 8V - 17V$<br>$V_{EE1}$ and $V_{EE2}$ is connected by the same voltage.   |              |                  |                           |                           |
| 74(72), 7(5)<br>76(74), 5(3)<br>77(75), 4(2)<br>75(73), 6(4) | $V_{0L}$ , $V_{0R}$<br>$V_{2L}$ , $V_{2R}$<br>$V_{3L}$ , $V_{3R}$<br>$V_{5L}$ , $V_{5R}$ | Power        | Bias supply voltage terminals to drive the LCD.<br><table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Select Level</th> <th>Non-Select Level</th> </tr> </thead> <tbody> <tr> <td><math>V_{0L(R)}</math>, <math>V_{5L(R)}</math></td> <td><math>V_{2L(R)}</math>, <math>V_{3L(R)}</math></td> </tr> </tbody> </table><br>$V_{0L}$ and $V_{0R}$ ( $V_{2L}$ & $V_{2R}$ , $V_{3L}$ & $V_{3R}$ , $V_{5L}$ & $V_{5R}$ ) should be connected by the same voltage. | Select Level | Non-Select Level | $V_{0L(R)}$ , $V_{5L(R)}$ | $V_{2L(R)}$ , $V_{3L(R)}$ |
| Select Level   | Non-Select Level   |              |   |              |                  |                           |                           |
| $V_{0L(R)}$ , $V_{5L(R)}$                                    | $V_{2L(R)}$ , $V_{3L(R)}$  |              |   |              |                  |                           |                           |
| 92(89)<br>91(87)<br>90(86)                                   | CS1B<br>CS2B<br>CS3  | Input        | Chip selection<br>In order to interface data for input or output, the terminals have to be CS1B = L, CS2B = L, and CS3 = H.   |              |                  |                           |                           |
| 2(100)   | M  | Input        | Alternating signal input for LCD driving.   |              |                  |                           |                           |
| 1(99)  | ADC  | Input        | Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output.<br>ADC = H $\rightarrow$ Y0: S1 - Y63: S64<br>ADC = L $\rightarrow$ Y0: S64 - Y63: S1  |              |                  |                           |                           |
| 100(98)  | FRM  | Input        | Synchronous control signal.<br>Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high.   |              |                  |                           |                           |
| 99(97)   | E  | Input        | Enable signal.<br>Write mode (R/W = L) $\rightarrow$ data of DB<0:7> is latched at the falling edge of E.<br>Read mode (R/W = H) $\rightarrow$ DB<0:7> appears the reading data while E is at high level.   |              |                  |                           |                           |
| 98(96)<br>97(95)   | CLK1<br>CLK2   | Input        | 2 phase clock signal for internal operation.<br>Used to execute operations for input/output of display RAM data and others.   |              |                  |                           |                           |
| 96(94)   | CL   | Input        | Display synchronous signal.<br>Display data is latched at rising time of the CL signal and increments the Z-address counter at the CL falling time.   |              |                  |                           |                           |
| 95(93)   | RS   | Input        | Data or Instruction.<br>RS = H $\rightarrow$ DB<0:7>: Display RAM data<br>RS = L $\rightarrow$ DB<0:7>: Instruction data  |              |                  |                           |                           |

Table 1. Pin Description (Continued)

| Pin Number<br>QFP(TQFP)  | Symbol  | Input/Output   | Description   |   |      |              |   |   |                |   |                |   |   |                |   |                |
|--------------------------|---------|----------------|---|---|------|--------------|---|---|----------------|---|----------------|---|---|----------------|---|----------------|
| 94(92)                   | R/W     | Input          | Read or Write.<br>R/W = H → Data appears at DB<0:7> and can be read by the CPU while E = H, CS1B = L, CS2B = L and CS3 = H .<br>R/W = L → Display data DB<0:7> can be written at falling of E when CS1B = L, CS2B = L and CS3 = H.  |   |      |              |   |   |                |   |                |   |   |                |   |                |
| 79-86<br>(77-84)         | DB0-DB7 | Input/Output   | Data bus.<br>There state I/O common terminal.   |   |      |              |   |   |                |   |                |   |   |                |   |                |
| 72-9<br>(70-7)           | S1-S64  | Output         | LCD segment driver output.<br>Display RAM data 1: On<br>Display RAM data 0: Off (relation of display RAM data & M) <table border="1" data-bbox="699 808 1153 999"> <thead> <tr> <th>M</th> <th>Data</th> <th>Output Level</th> </tr> </thead> <tbody> <tr> <td rowspan="2">L</td> <td>L</td> <td>V<sub>2</sub></td> </tr> <tr> <td>H</td> <td>V<sub>0</sub></td> </tr> <tr> <td rowspan="2">H</td> <td>L</td> <td>V<sub>3</sub></td> </tr> <tr> <td>H</td> <td>V<sub>5</sub></td> </tr> </tbody> </table> | M | Data | Output Level | L | L | V <sub>2</sub> | H | V <sub>0</sub> | H | L | V <sub>3</sub> | H | V <sub>5</sub> |
| M                        | Data    | Output Level   |   |   |      |              |   |   |                |   |                |   |   |                |   |                |
| L                        | L       | V <sub>2</sub> |   |   |      |              |   |   |                |   |                |   |   |                |   |                |
|                          | H       | V <sub>0</sub> |   |   |      |              |   |   |                |   |                |   |   |                |   |                |
| H                        | L       | V <sub>3</sub> |   |   |      |              |   |   |                |   |                |   |   |                |   |                |
|                          | H       | V <sub>5</sub> |   |   |      |              |   |   |                |   |                |   |   |                |   |                |
| 93(91)                   | RSTB    | Input          | Reset signal.<br>When RSTB=L,<br>- ON/OFF register becomes set by 0. (display off)<br>- Display start line register becomes set by 0 (Z-address 0 set, display from line 0)<br>After releasing reset, this condition can be changed only by instruction.  |   |      |              |   |   |                |   |                |   |   |                |   |                |
| 87(85), 88(88)<br>89(90) | NC      |                | No connection. (open)   |   |      |              |   |   |                |   |                |   |   |                |   |                |

**MAXIMUM ABSOLUTE LIMIT**

| Characteristic        | Symbol    | Value                         | Unit | Note     |
|-----------------------|-----------|-------------------------------|------|----------|
| Operating voltage     | $V_{DD}$  | -0.3 to +7.0                  | V    | (1)      |
| Supply voltage        | $V_{EE}$  | $V_{DD}-19.0$ to $V_{DD}+0.3$ | V    | (4)      |
| Driver supply voltage | $V_B$     | -0.3 to $V_{DD}+0.3$          | V    | (1), (3) |
|                       | $V_{LCD}$ | $V_{EE}-0.3$ to $V_{DD}+0.3$  | V    | (2)      |
| Operating temperature | $T_{OPR}$ | -30 to +85                    | °C   |          |
| Storage temperature   | $T_{STG}$ | -55 to +125                   | °C   |          |

**NOTES:**

1. Based on  $V_{SS} = 0V$ .
2. Applies the same supply voltage to  $V_{EE1}$  and  $V_{EE2}$ .  $V_{LCD} = V_{DD} - V_{EE}$ .
3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0 - DB7.
4. Applies to V0L(R), V2L(R), V3L(R) and V5L(R).  
Voltage level:  $V_{DD} \geq V0L = V0R \geq V2L = V2R \geq V3L = V3R \geq V5L = V5R \geq V_{EE}$ .

## ELECTRICAL CHARACTERISTICS

### DC CHARACTERISTICS

( $V_{DD} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $V_{DD} - V_{EE} = 8$  to  $17V$ ,  $T_a = -30$  to  $+85^\circ C$ )

| Characteristic                 | Symbol    | Condition   | Min         | Typ | Max         | Unit      | Note |
|--------------------------------|-----------|---|-------------|-----|-------------|-----------|------|
| Input high voltage             | $V_{IH1}$ | –   | $0.7V_{DD}$ | –   | $V_{DD}$    | V         | (1)  |
|                                | $V_{IH2}$ | –   | 2.0         | –   | $V_{DD}$    | V         | (2)  |
| Input low voltage              | $V_{IL1}$ | –   | 0           | –   | $0.3V_{DD}$ | V         | (1)  |
|                                | $V_{IL2}$ | –   | 0           | –   | 0.8         | V         | (2)  |
| Output high voltage            | $V_{OH}$  | $I_{OH} = -200\mu A$                              | 2.4         | –   | –           | V         | (3)  |
| Output low voltage             | $V_{OL}$  | $I_{OL} = 1.6mA$                                  | –           | –   | 0.4         | V         | (3)  |
| Input leakage current          | $I_{LKG}$ | $V_{IN} = V_{SS} - V_{DD}$                        | -1.0        | –   | 1.0         | $\mu A$   | (4)  |
| Three-state(off) input current | $I_{TSL}$ | $V_{IN} = V_{SS} - V_{DD}$                        | -5.0        | –   | 5.0         | $\mu A$   | (5)  |
| Driver input leakage current   | $I_{DIL}$ | $V_{IN} = V_{EE} - V_{DD}$                        | -2.0        | –   | 2.0         | $\mu A$   | (6)  |
| Operating current              | $I_{DD1}$ | During display                                    | –           | –   | 100         | $\mu A$   | (7)  |
|                                | $I_{DD2}$ | During access<br>Access cycle = 1MHz              | –           | –   | 500         | $\mu A$   | (7)  |
| On resistance                  | $R_{ON}$  | $V_{DD} - V_{EE} = 15V$<br>$I_{LOAD} = \pm 0.1mA$ | –           | –   | 7.5         | $K\Omega$ | (8)  |

#### NOTES:

1. CL, FRM, M, RSTB, CLK1, CLK2
2. CS1B, CS2B, CS3, E, R/W, RS, DB0 - DB7
3. DB0 - DB7
4. Except DB0 - DB7
5. DB0 - DB7 at high impedance
6. V0L(R), V2L(R), V3L(R), V5L(R)
7. 1/64 duty, FCLK = 250kHz, frame frequency = 70HZ, output: no load
8.  $V_{DD} - V_{EE} = 15.5V$   
 $V0L(R) > V2L(R) = V_{DD} - 2/7 (V_{DD} - V_{EE}) > V3L(R) = V_{EE} + 2/7 (V_{DD} - V_{EE}) > V5L(R)$



AC CHARACTERISTICS ( $V_{DD} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = -30$  to  $+85^\circ C$ )

## Clock Timing

| Characteristic             | Symbol    | Min  | Typ | Max | Unit    |
|----------------------------|-----------|------|-----|-----|---------|
| CLK1, CLK2 cycle time      | $t_{CY}$  | 2.5  | –   | 20  | $\mu s$ |
| CLK1 "low" level width     | $t_{WL1}$ | 625  | –   | –   | ns      |
| CLK2 "low" level width     | $t_{WL2}$ | 625  | –   | –   |         |
| CLK1 "high" level width    | $t_{WH1}$ | 1875 | –   | –   |         |
| CLK2 "high" level width    | $t_{WH2}$ | 1875 | –   | –   |         |
| CLK1-CLK2 phase difference | $t_{D12}$ | 625  | –   | –   |         |
| CLK2-CLK1 phase difference | $t_{D21}$ | 625  | –   | –   |         |
| CLK1, CLK2 rise time       | $t_R$     | –    | –   | 150 |         |
| CLK1, CLK2 fall time       | $t_F$     | –    | –   | 150 |         |

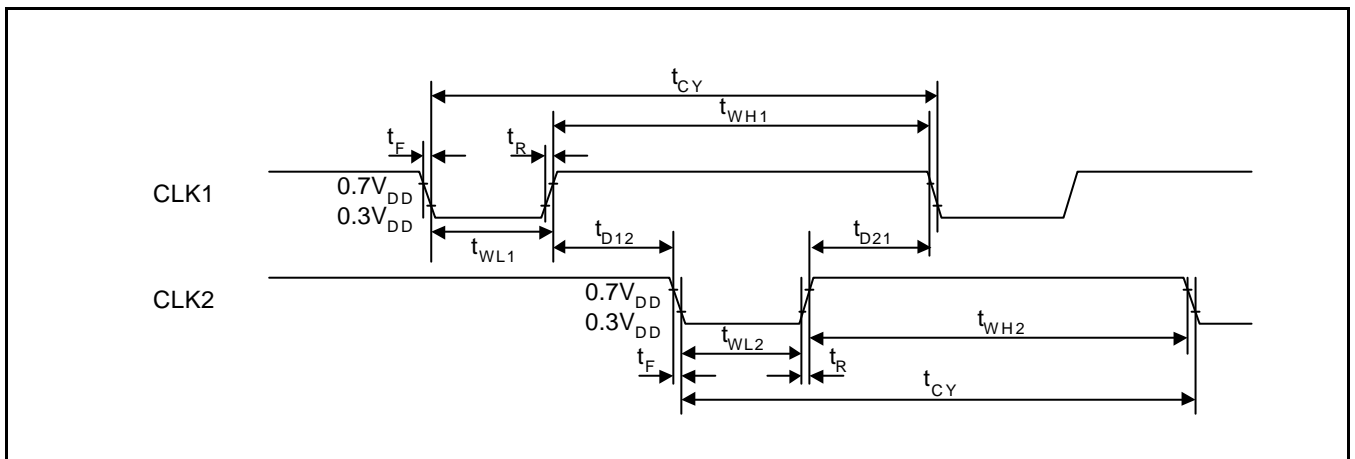


Figure 1. External Clock Waveform

## Display Control Timing

| Characteristic        | Symbol   | Min | Typ | Max | Unit |
|-----------------------|----------|-----|-----|-----|------|
| FRM delay time        | $t_{DF}$ | -2  | -   | +2  | us   |
| M delay time          | $t_{DM}$ | -2  | -   | +2  | us   |
| CL "low" level width  | $t_{WL}$ | 35  | -   | -   | us   |
| CL "high" level width | $t_{WH}$ | 35  | -   | -   | us   |

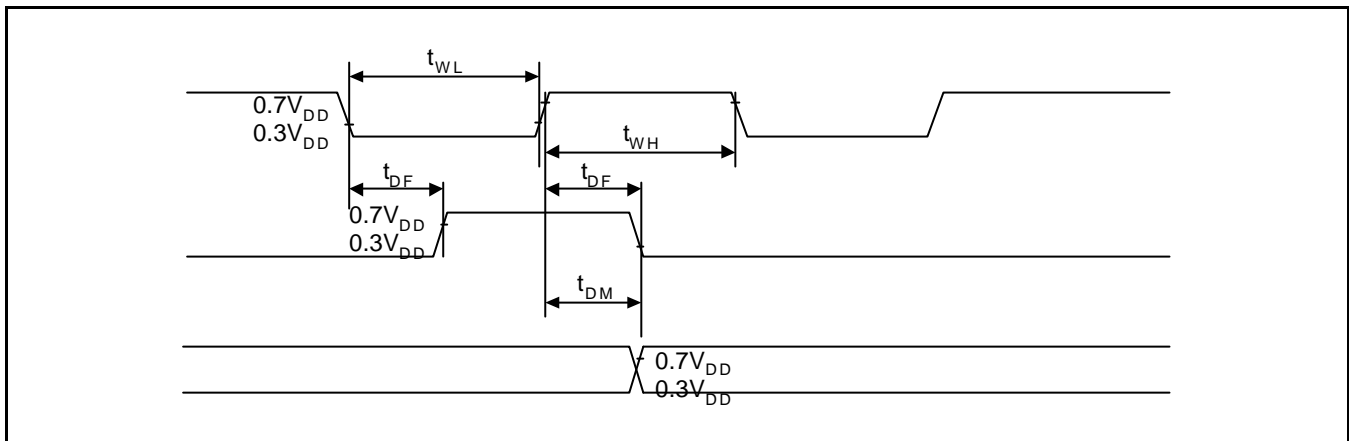


Figure 2. Display Control Waveform

MPU Interface

| Characteristic         | Symbol    | Min  | Typ | Max | Unit |
|------------------------|-----------|------|-----|-----|------|
| E cycle                | $t_C$     | 1000 | –   | –   | ns   |
| E high level width     | $t_{WH}$  | 450  | –   | –   | ns   |
| E low level width      | $t_{WL}$  | 450  | –   | –   | ns   |
| E rise time            | $t_R$     | –    | –   | 25  | ns   |
| E fall time            | $t_F$     | –    | –   | 25  | ns   |
| Address set-up time    | $t_{ASU}$ | 140  | –   | –   | ns   |
| Address hold time      | $t_{AH}$  | 10   | –   | –   | ns   |
| Data set-up time       | $t_{DSU}$ | 200  | –   | –   | ns   |
| Data delay time        | $t_D$     | –    | –   | 320 | ns   |
| Data hold time (write) | $t_{DHW}$ | 10   | –   | –   | ns   |
| Data hold time (read)  | $t_{DHR}$ | 20   | –   | –   | ns   |

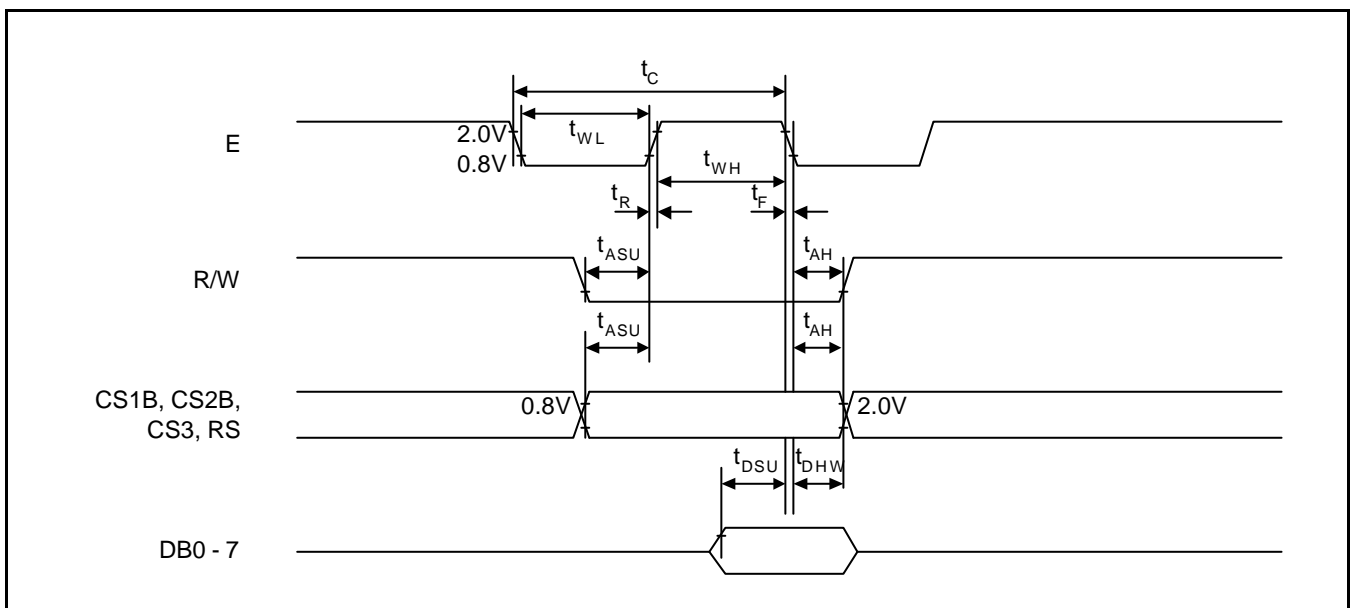


Figure 3. MPU Write Timing

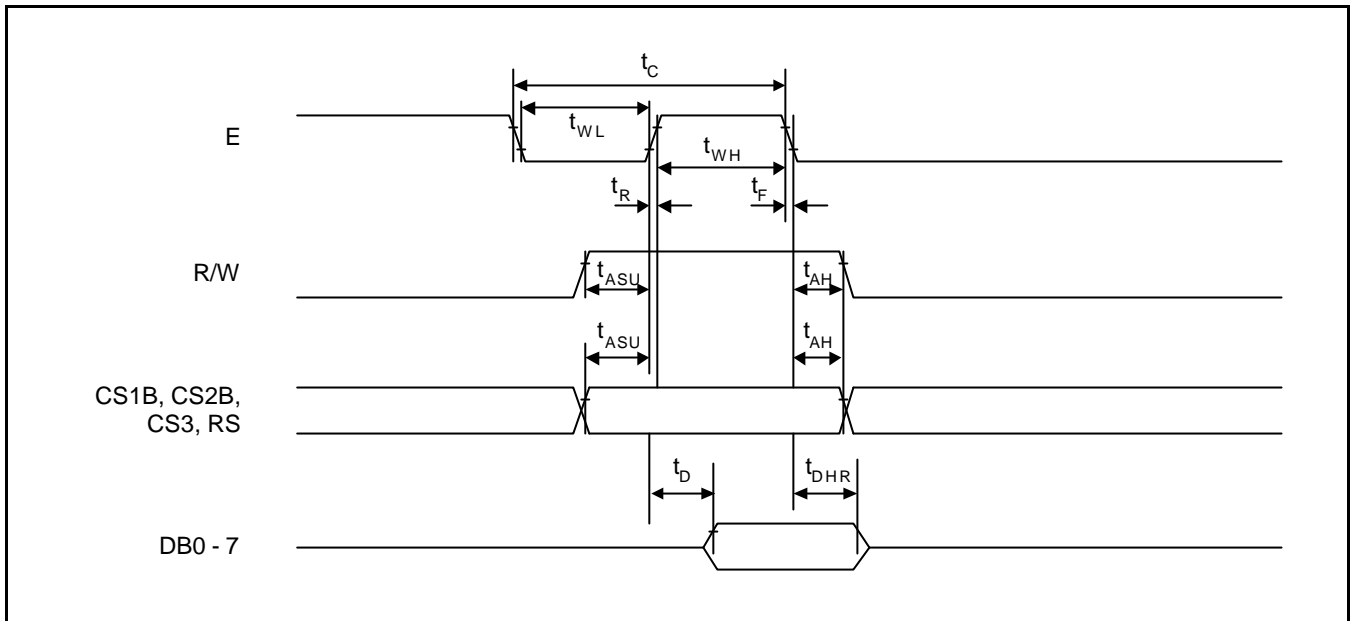


Figure 4. MPU Read Timing

## OPERATING PRINCIPLES AND METHODS

### I/O BUFFER

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

### INPUT REGISTER

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM. When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then Writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

### OUTPUT REGISTER

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS = H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W = H, RS = L, status data (busy check) can read out. To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

| RS | R/W | Function   |
|----|-----|--|
| L  | L   | Instruction  |
|    | H   | Status read (busy check)                             |
| H  | L   | Data write (from input register to display data RAM) |
|    | H   | Data read (from display data RAM to output register) |

## RESET

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.

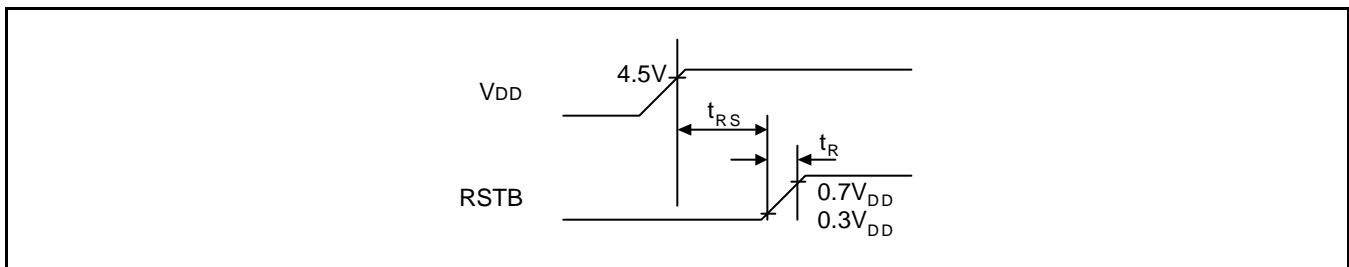
When RSTB becomes low, following procedure is occurred.

- Display off
- Display start line register become set by 0. (Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RSTB) and DB7 = 0 (ready) by status read instruction. The Conditions of power supply at initial power up are shown in Table 2.

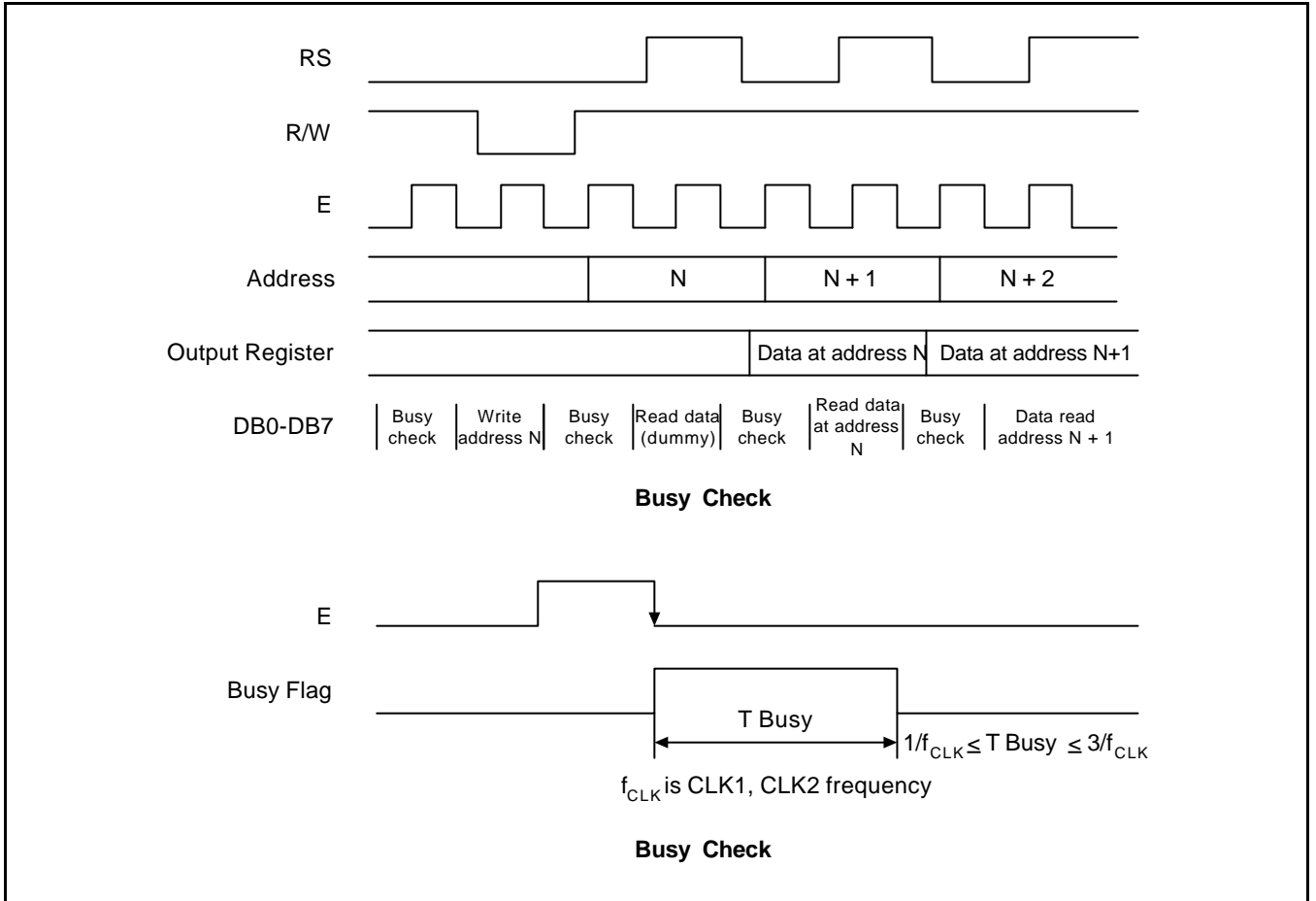
**Table 2. Power Supply Initial Conditions**

| Item       | Symbol   | Min | Typ | Max | Unit |
|------------|----------|-----|-----|-----|------|
| Reset time | $t_{RS}$ | 1.0 | —   | —   | us   |
| Rise time  | $t_R$    | —   | —   | 200 | ns   |



**Busy Flag**

Busy Flag indicates that S6B0108 is operating or no operating. When busy flag is high, S6B0108 is in internal operating. When busy flag is low, S6B0108 can accept the data or instruction. DB7 indicates busy flag of the S6B0108.



### Display ON/OFF Flip - Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

### X Page Register

X page register designates pages of the internal display data RAM. Count function is not available. An address is set by instruction.

### Y Address Counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

### Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

- ADC = H → Y-address 0:S1 - Y address 63:S64
- ADC = L → Y-address 0:S64 - Y address 63:S1

ADC terminal connect the  $V_{DD}$  or  $V_{SS}$ .

### Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display. Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter. It is used for scrolling of the liquid crystal display screen.



## DISPLAY CONTROL INSTRUCTION

The display control instructions control the internal state of the S6B0108. Instruction is received from MPU to S6B0108 for the display control. The following table shows various instructions.

| Instruction                    | RS | R/W | DB7        | DB6 | DB5                         | DB4   | DB3 | DB2          | DB1 | DB0  | Function  |
|--------------------------------|----|-----|------------|-----|-----------------------------|-------|-----|--------------|-----|--|---|
| Display on/off                 | L  | L   | L          | L   | H                           | H     | H   | H            | H   | L/H  | Controls the display on or off. Internal status and display RAM data is not affected. L: OFF, H: ON                       |
| Set address (Y address)        | L  | L   | L          | H   | Y address (0 - 63)          |       |     |              |     | Sets the Y address in the Y address counter.                       |   |
| Set page (X address)           | L  | L   | H          | L   | H                           | H     | H   | Page (0 - 7) |     | Sets the X address at the X address register.                      |   |
| Display start line (Z address) | L  | L   | H          | H   | Display start line (0 - 63) |       |     |              |     | Indicates the display data RAM displayed at the top of the screen. |   |
| Status read                    | L  | H   | Busy       | L   | On/Off                      | Reset | L   | L            | L   | L  | Read status.<br>BUSY L: Ready<br>H: In operation<br>ON/OFF L: Display ON<br>H: Display OFF<br>RESET L: Normal<br>H: Reset |
| Write display data             | H  | L   | Write data |     |                             |       |     |              |     |  | Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.          |
| Read display data              | H  | H   | Read data  |     |                             |       |     |              |     |  | Reads data (DB0:7) from display data RAM to the data bus.   |

**DISPLAY ON/OFF**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | 1   | 1   | 1   | 1   | D   |

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

**SET ADDRESS (Y ADDRESS)**

| S | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0   | 0   | 1   | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Y address (AC0 - AC5) of the display data RAM is set in the Y address counter. An address is set by instruction and increased by 1 automatically by read or write operations of display data.

**SET PAGE (X ADDRESS)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 1   | 0   | 1   | 1   | 1   | AC2 | AC1 | AC0 |

X address(AC0 - AC2) of the display data RAM is set in the X address register. Writing or reading to or from MPU is executed in this specified page until the next page is set.

**DISPLAY START LINE (Z ADDRESS)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 1   | 1   | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Z address (AC0 - AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen. When the display duty cycle is 1/64 or others(1/32 - 1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

**STATUS READ**

| RS | R/W | DB7  | DB6 | DB5    | DB4   | DB3 | DB2 | DB1 | DB0 |
|----|-----|------|-----|--------|-------|-----|-----|-----|-----|
| 0  | 1   | BUSY | 0   | ON/OFF | RESET | 0   | 0   | 0   | 0   |

- **BUSY**  
When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.  
When BUSY is 0, the Chip is ready to accept any instructions.
- **ON/OFF**  
When ON/OFF is 1, the display is off.  
When ON/OFF is 0, the display is on.
- **RESET**  
When RESET is 1, the system is being initialized.  
In this condition, no instructions except status read can be accepted.  
When RESET is 0, initializing has finished and the system is in the usual operation condition.

**WRITE DISPLAY DATA**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

Writes data (D0 - D7) into the display data RAM. After writing instruction, Y address is increased by 1 automatically.

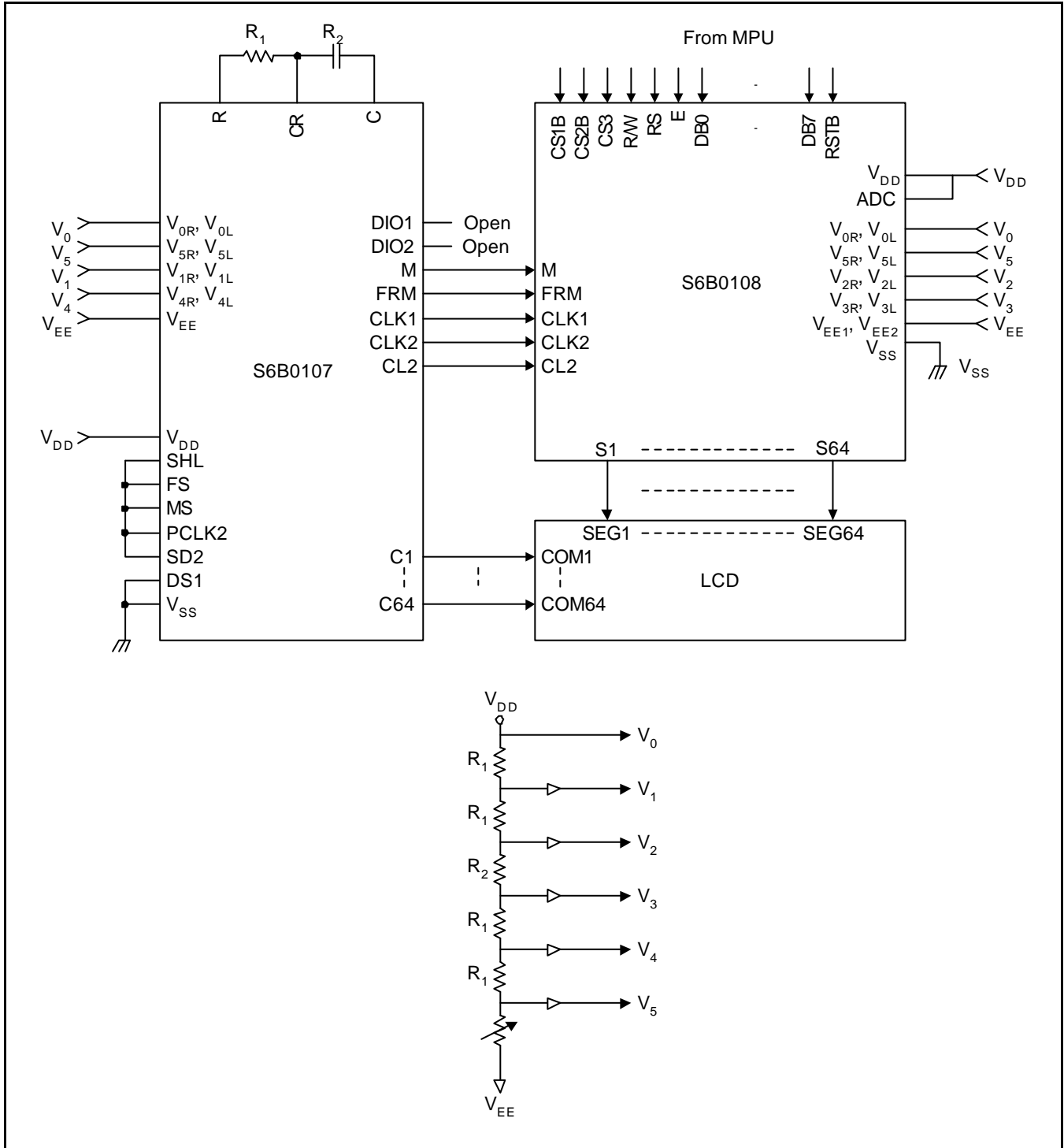
**READ DISPLAY DATA**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 1   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

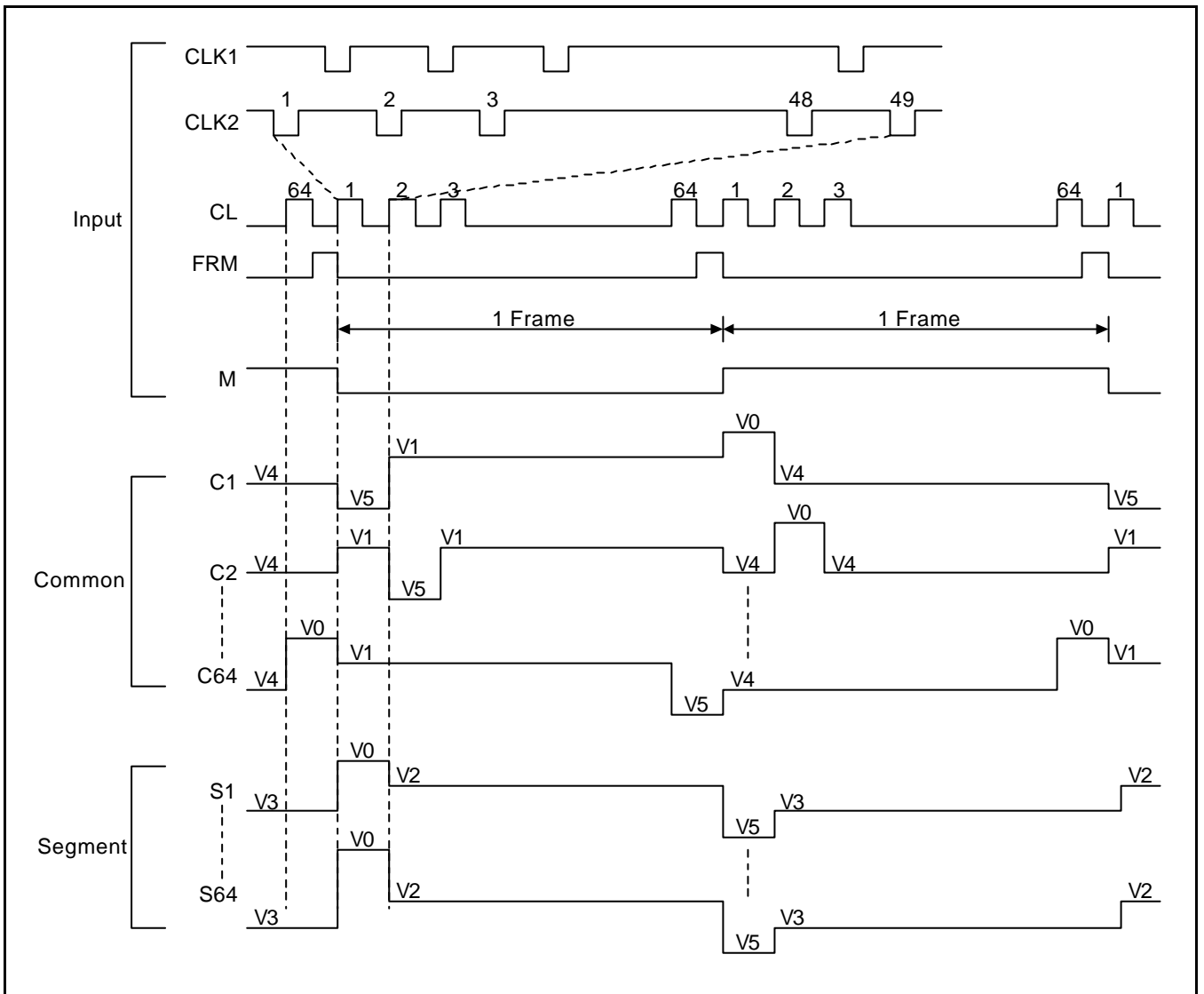
Reads data (D0 - D7) from the display data RAM. After reading instruction, Y address is increased by 1 automatically.

APPLICATION CIRCUIT

1/64 DUTY COMMON DRIVER (S6B0107) INTERFACE CIRCUIT



TIMING DIAGRAM (1/64 DUTY)



LCD PANEL INTERFACE APPLICATION CIRCUIT

